

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	APPD DATE
			2010-07-23

SCHEM, MLB, K16


07/23/2010

Page	Contents	Sync	Date
1	Table of Contents	N/A	N/A
2	System Block Diagram	ALAN_DAI	02/26/2010
3	Power Block Diagram	MARTIN_YEH	2/25/2010
4	BOM Configuration	K6_MLB	12/11/2009
5	K16 BOM Variants	N/A	N/A
6	Revision History	N/A	N/A
7	Functional Test / No Test	(K99_MLB)	(02/16/2010)
8	Power Aliases	(K99_MLB)	(02/11/2010)
9	Signal Aliases	(MASTER)	(MASTER)
10	CPU FSB	K99_MLB	04/08/2010
11	CPU Power & Ground	K99_MLB	04/08/2010
12	CPU Decoupling & VID	(K99_MLB)	(02/11/2010)
13	eXtended Debug Port (Micro-XDP)	K99_MLB	03/01/2010
14	MCP CPU Interface	K99_MLB	04/08/2010
15	MCP Memory Interface	K99_MLB	04/08/2010
16	MCP PCIe Interfaces	K99_MLB	04/08/2010
17	MCP Graphics	K99_MLB	04/08/2010
18	MCP SATA, USB & Ethernet	K99_MLB	04/08/2010
19	MCP HDA, LPC & MISC	K99_MLB	04/08/2010
20	MCP Power & Ground	K99_MLB	04/08/2010
21	MCP89 Memory Rail Gating	K99_MLB	04/08/2010
22	MCP89 GFX Core Rail Gating	K99_MLB	04/08/2010
23	MCP Standard Decoupling	K99_MLB	04/08/2010
24	MCP Graphics Support	K99_MLB	04/08/2010
25	SB Misc	(K99_MLB)	(02/11/2010)
26	DDR3 DRAM Channel A (0-31)	K99_MLB	04/08/2010
27	DDR3 DRAM Channel A (32-63)	K99_MLB	04/08/2010
28	DDR3 DRAM Channel B (0-31)	K99_MLB	04/08/2010
29	DDR3 DRAM Channel B (32-63)	K99_MLB	04/08/2010
30	DDR BYPASSING 1	K99_MLB	04/08/2010
31	DDR BYPASSING 2	K99_MLB	04/08/2010
32	Memory Active Termination	K99_MLB	04/08/2010
33	FSB/DDR3 Vref Margining	K99_MLB	04/08/2010
34	X21 WIRELESS CONNECTOR	K99_MLB	04/08/2010
35	SATA CONNECTOR	K99_MLB	04/08/2010
36	External USB Connectors	K99_MLB	03/01/2010
37	Left I/O (LIO) Connector	(MASTER)	(MASTER)
38	SecureDigital Card Reader	(MASTER)	(MASTER)

Page	Contents	Sync	Date
39	SMC	K16_MLB	06/01/2010
40	SMC Support	(K99_MLB)	(03/01/2010)
41	LPC+SPI Debug Connector	K99_MLB	04/08/2010
42	K16/K99 SMus Connections	K99_MLB	07/23/2010
43	Voltage & Current Sensing	K99_MLB	04/08/2010
44	Current Sensing	K99_MLB	04/08/2010
45	Thermal Sensors	K99_MLB	04/08/2010
46	Fan	K99_MLB	04/08/2010
47	WELLSPRING 1	K99_MLB	04/08/2010
48	SPI ROM	K99_MLB	04/08/2010
49	AUDIO0: SPEAKER AMP	K99_MLB	04/08/2010
50	DC-In & Battery Connectors	(MASTER)	(MASTER)
51	PBus Supply & Battery Charger	(K99_MLB)	(02/16/2010)
52	5V / 3.3V Power Supply	K99_MLB	04/08/2010
53	1.5V/1.35V LVDDR3 Supply	K16_MLB	06/01/2010
54	IMVP6 CPU VCore Regulator	(K99_MLB)	(02/16/2010)
55	MCP VCore Regulator	(K99_MLB)	(02/11/2010)
56	CPUVTT (1.05V) Power Supply	(K99_MLB)	(03/01/2010)
57	Misc Power Supplies	K99_MLB	04/08/2010
58	Power Sequencing	K99_MLB	04/08/2010
59	Power FETs	K99_MLB	04/08/2010
60	Internal DisplayPort Connector	K99_MLB	07/23/2010
61	External DisplayPort Support	K99_MLB	04/08/2010
62	DisplayPort Connector	K16_MLB	06/01/2010
63	LCD Backlight Driver	(K99_MLB)	(03/01/2010)
64	LCD Backlight Support	K99_MLB	04/08/2010
65	Additional CPU/GPU Decoupling	K99_MLB	05/18/2010
66	CPU/FSB Constraints	K99_MLB	04/08/2010
67	Memory Constraints	K99_MLB	04/08/2010
68	MCP Constraints 1	K99_MLB	04/08/2010
69	MCP Constraints 2	K99_MLB	04/08/2010
70	Ethernet Constraints	K99_MLB	04/08/2010
71	SMC Constraints	K99_MLB	04/08/2010
72	K16/K99 Specific Constraints	T27_MLB	09/08/2009
73	K99 RULE DEFINITIONS	K99_MLB	04/08/2010
74	Acoustic Cap BOM Config Tables	K16_MLB	06/01/2010

Schematic / PCB #'s

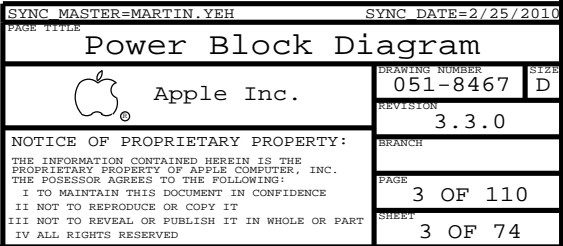
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8467	1	SCHEM,MLB,K16	SCH	CRITICAL	
820-2838	1	PCBF,MLB,K16	PCB	CRITICAL	

DRAWING TITLE	
SCHEM, MLB, K16	
 Apple Inc.	DRAWING NUMBER
	051-8467
	SIZE
	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I LI NOT TO REPRODUCE OR COPY IT I LI NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I LI ALL RIGHTS RESERVED	REVISION
	3.3.0
	BRANCH
	PAGE
	1 OF 110
	SHEET
	1 OF 74



SYNC MASTER-ALAN.DAI		SYNC DATE=02/26/2010	
PAGE TITLE		SIZE	
System Block Diagram			
DRAWING NUMBER		051-8467	
D		D	
REVISION		3.3.0	
BRANCH			
PAGE		2 OF 110	
SHEET		2 OF 74	

www.teknisi-indonesia.com



VENDOR	CFG 0	CFG 1
HYNIX	0	0
SAMSUNG	0	1
MICRON	1	0
ELPIDA	1	1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3820	1	IC,MCP890-A01,24,5MHX24,5MH,1244PCBGA	U1400	CRITICAL	MCP890:A01
337S3868	1	IC,MCP890-A02,24,5MHX24,5MH,1244PCBGA	U1400	CRITICAL	MCP890:A02
337S3938	1	IC,MCP890-A03,24,5MHX24,5MH,1244PCBGA	U1400	CRITICAL	MCP890:A03

BOM GROUP	BOM OPTIONS
K16_COMMON	COMMON,ALTERNATE,PROJ:K16,K16_MISC,MCP89U:A03,K16_DEBUG:ENG,K16_PROGPARTS,SPI:41MHZ,LVDDR3:YES,WLAN_PCTL:HW,IPD_5V:S5_INT,IPD_3V3:S5
K16_MISC	DP_BSD,DP_PWR:SMC,VFRQ:SLP53,HVDDLDO:FIXED,MCPHVD:P2V5,MCPPLL_R:REG,S0PGOOD_BJT,ISL6259_SCREENED:YES,DPI2C:SMC
K16_PROGPARTS	BOOTROM:UNLOCKED,SMC:PROG
K16_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,LPCPLUS,VREFMRGN:YES,EFI_DEBUG,S0PGOOD_ISL,MCPPLL_LDO,S3_S0_LED
K16_DEVEL:PVT	LPCPLUS
K16_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG:YES,XDP
K16_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
K16_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_2GB	DRAM_CFG0:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_2GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_4GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:MICRON_4GB
CAPS:SS	SS_CAP_2_2UF,SS_CAP_10UF,SS_CAP_1UF,SS_CAP_22UF
CAPS:MU	MU_CAP_2_2UF,MU_CAP_10UF,MU_CAP_1UF,MU_CAP_22UF
CAPS:TY	TY_CAP_2_2UF,TY_CAP_10UF,TY_CAP_1UF,TY_CAP_22UF

338S0563	1	IC, SMC, HS8/2117, 9X9MM, TLP, HF	U4900	CRITICAL	SMC:BLANK
335S0610	1	IC, FLASH, SPI, 32MBIT, 3.3V, 86MHZ, 8-SOP	U6100	CRITICAL	BOOTROM:BLANK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
-------------	------------------------------	------------	---------	-----------

	8	7	6	5	4	3	2	1										
	BOM Variants			Bar Code Labels / EEE #'s														
	BOM NUMBER	BOM NAME	BOM OPTIONS	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION									
D	639-1070	PCBA,MLB,1.86GHZ HY 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWQ,CAPS:MU,DDR3:HYNIX_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWM]	CRITICAL	EEEE:DCWM									
	639-0837	PCBA,MLB,1.86GHZ,HY 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXW,CAPS:SS,DDR3:HYNIX_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWN]	CRITICAL	EEEE:DCWN									
	639-1096	PCBA,MLB,1.86GHZ HY 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXN,CAPS:TY,DDR3:HYNIX_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWP]	CRITICAL	EEEE:DCWP									
	639-1101	PCBA,MLB,1.86GHZ HY 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXV,CAPS:MU,DDR3:HYNIX_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWQ]	CRITICAL	EEEE:DCWQ									
	639-1098	PCBA,MLB,1.86GHZ HY 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXQ,CAPS:SS,DDR3:HYNIX_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWR]	CRITICAL	EEEE:DCWR									
	639-1068	PCBA,MLB,1.86GHZ HY 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWN,CAPS:TY,DDR3:HYNIX_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWT]	CRITICAL	EEEE:DCWT									
	639-1083	PCBA,MLB,1.86GHZ MI 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX6,CAPS:MU,DDR3:MICRON_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWV]	CRITICAL	EEEE:DCWV									
	639-1078	PCBA,MLB,1.86GHZ MI 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX1,CAPS:SS,DDR3:MICRON_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWW]	CRITICAL	EEEE:DCWW									
	639-1090	PCBA,MLB,1.86GHZ MI 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXG,CAPS:TY,DDR3:MICRON_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWX]	CRITICAL	EEEE:DCWX									
	639-1088	PCBA,MLB,1.86GHZ MI 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXD,CAPS:MU,DDR3:MICRON_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWY]	CRITICAL	EEEE:DCWY									
C	639-1067	PCBA,MLB,1.86GHZ MI 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWM,CAPS:SS,DDR3:MICRON_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX0]	CRITICAL	EEEE:DCX0									
	639-1077	PCBA,MLB,1.86GHZ MI 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX0,CAPS:TY,DDR3:MICRON_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX1]	CRITICAL	EEEE:DCX1									
	639-1080	PCBA,MLB,1.86GHZ SA 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX2,CAPS:MU,DDR3:SAMSUNG_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX2]	CRITICAL	EEEE:DCX2									
	639-1095	PCBA,MLB,1.86GHZ SA 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXM,CAPS:SS,DDR3:SAMSUNG_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX3]	CRITICAL	EEEE:DCX3									
	639-1071	PCBA,MLB,1.86GHZ SA 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWR,CAPS:TY,DDR3:SAMSUNG_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX4]	CRITICAL	EEEE:DCX4									
	639-1097	PCBA,MLB,1.86GHZ SA 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXP,CAPS:MU,DDR3:SAMSUNG_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX5]	CRITICAL	EEEE:DCX5									
	639-1084	PCBA,MLB,1.86GHZ SA 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX7,CAPS:SS,DDR3:SAMSUNG_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX6]	CRITICAL	EEEE:DCX6									
	639-1091	PCBA,MLB,1.86GHZ SA 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXH,CAPS:TY,DDR3:SAMSUNG_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX7]	CRITICAL	EEEE:DCX7									
	639-1092	PCBA,MLB,2.13GHZ HY 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXJ,CAPS:MU,DDR3:HYNIX_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX8]	CRITICAL	EEEE:DCX8									
	639-1082	PCBA,MLB,2.13GHZ,HY 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX5,CAPS:SS,DDR3:HYNIX_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX9]	CRITICAL	EEEE:DCX9									
B	639-1085	PCBA,MLB,2.13GHZ HY 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX8,CAPS:TY,DDR3:HYNIX_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXC]	CRITICAL	EEEE:DCXC									
	639-1089	PCBA,MLB,2.13GHZ HY 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXF,CAPS:MU,DDR3:HYNIX_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXD]	CRITICAL	EEEE:DCXD									
	639-1075	PCBA,MLB,2.13GHZ HY 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWX,CAPS:SS,DDR3:HYNIX_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXF]	CRITICAL	EEEE:DCXF									
	639-1079	PCBA,MLB,2.13GHZ HY 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX2,CAPS:TY,DDR3:HYNIX_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXG]	CRITICAL	EEEE:DCXG									
	639-1099	PCBA,MLB,2.13GHZ MI 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXR,CAPS:MU,DDR3:MICRON_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXH]	CRITICAL	EEEE:DCXH									
	639-1087	PCBA,MLB,2.13GHZ MI 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXC,CAPS:SS,DDR3:MICRON_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXJ]	CRITICAL	EEEE:DCXJ									
	639-1069	PCBA,MLB,2.13GHZ MI 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWP,CAPS:TY,DDR3:MICRON_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXK]	CRITICAL	EEEE:DCXK									
	639-1100	PCBA,MLB,2.13GHZ MI 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXT,CAPS:MU,DDR3:MICRON_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXL]	CRITICAL	EEEE:DCXL									
	639-1093	PCBA,MLB,2.13GHZ MI 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXK,CAPS:SS,DDR3:MICRON_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXM]	CRITICAL	EEEE:DCXM									
	639-1076	PCBA,MLB,2.13GHZ MI 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWY,CAPS:TY,DDR3:MICRON_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXN]	CRITICAL	EEEE:DCXN									
A	639-1074	PCBA,MLB,2.13GHZ SA 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWW,CAPS:MU,DDR3:SAMSUNG_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXP]	CRITICAL	EEEE:DCXP									
	639-1072	PCBA,MLB,2.13GHZ SA 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWT,CAPS:SS,DDR3:SAMSUNG_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXQ]	CRITICAL	EEEE:DCXQ									
	639-1086	PCBA,MLB,2.13GHZ SA 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX9,CAPS:TY,DDR3:SAMSUNG_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXR]	CRITICAL	EEEE:DCXR									
	639-1073	PCBA,MLB,2.13GHZ SA 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWV,CAPS:MU,DDR3:SAMSUNG_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXT]	CRITICAL	EEEE:DCXT									
	639-1081	PCBA,MLB,2.13GHZ SA 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX4,CAPS:SS,DDR3:SAMSUNG_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXV]	CRITICAL	EEEE:DCXV									
	639-1094	PCBA,MLB,2.13GHZ SA 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXL,CAPS:TY,DDR3:SAMSUNG_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXW]	CRITICAL	EEEE:DCXW									
	639-1450	PCBA,MLB,1.86GHZ EL 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG4W,CAPS:MU,DDR3:ELPIDA_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG4W]	CRITICAL	EEEE:DG4W									
	639-1451	PCBA,MLB,1.86GHZ EL 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG4Y,CAPS:SS,DDR3:ELPIDA_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG4Y]	CRITICAL	EEEE:DG4Y									
	639-1455	PCBA,MLB,1.86GHZ EL 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG53,CAPS:TY,DDR3:ELPIDA_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG53]	CRITICAL	EEEE:DG53									
	639-1453	PCBA,MLB,2.13GHZ EL 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG51,CAPS:MU,DDR3:ELPIDA_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG51]	CRITICAL	EEEE:DG51									
	639-1454	PCBA,MLB,2.13GHZ EL 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG52,CAPS:SS,DDR3:ELPIDA_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG52]	CRITICAL	EEEE:DG52									
	639-1452	PCBA,MLB,2.13GHZ EL 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG50,CAPS:TY,DDR3:ELPIDA_2GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG50]	CRITICAL	EEEE:DG50									
	639-1458	PCBA,MLB,1.86GHZ HY 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5P,CAPS:MU,DDR3:ELPIDA_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5P]	CRITICAL	EEEE:DG5P									
	639-1463	PCBA,MLB,1.86GHZ EL 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5W,CAPS:SS,DDR3:ELPIDA_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5W]	CRITICAL	EEEE:DG5W									
	639-1460	PCBA,MLB,1.86GHZ EL 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5T,CAPS:TY,DDR3:ELPIDA_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5T]	CRITICAL	EEEE:DG5T									
	639-1462	PCBA,MLB,2.13GHZ EL 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5Q,CAPS:MU,DDR3:ELPIDA_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5Q]	CRITICAL	EEEE:DG5Q									
	639-1459	PCBA,MLB,2.13GHZ EL 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5V,CAPS:SS,DDR3:ELPIDA_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5V]	CRITICAL	EEEE:DG5V									
	639-1461	PCBA,MLB,2.13GHZ EL 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5R,CAPS:TY,DDR3:ELPIDA_4GB	825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5R]	CRITICAL	EEEE:DG5R									
	607-6915	CMN PTS,PCBA,MLB,K16	K16_COMMON															
	085-1327	K16 MLB DEVELOPMENT BOM	K16_DEVEL:ENG															
	SAMSUNG			MURATA			TAIYO YUDEN											
	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
	138S0632	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	SS_CAP_2_2UF	138S0633	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	MU_CAP_2_2UF	138S0634	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	TY_CAP_2_2UF
	K16-Specific BOM Tables																	
	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION												
	337S3751	1	PDC,SLGAB,PRQ,1.86,17W,1066,ED,6M,BGA	U1000	CRITICAL	CPU:1.86GHZ												
	337S3758	1	PDC,SLGEQ,PRQ,2.13,17W,1066,ED,6M,BGA	U1000	CRITICAL	CPU:2.13GHZ												
	341T0276	1	IC ASSY,SMC EXTERNAL,K16	U4900	CRITICAL	SMC:PROG												
	341T0275	1	IC ASSY,EFI UNLOCKED,K16	U6100	CRITICAL	BOOTROM:UNLOCKED												
	341S2785	1	IC EFI ROM,PVT,LOCKED,K16	U6100	CRITICAL	BOOTROM:LOCKED												
	Sub-BOMs																	
	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION												
	085-1327	1	K16 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM												
	607-6915	1	CMN PTS,PCBA,MLB,K16	CMNPTS	CRITICAL	K16_CMNPTS												
	8	7	6	5	4	3	2	1	www.teknisi-indonesia.com									

SYNC MASTER=N/A

SYNC DATE=N/A

PAGE TITLE

K16 BOM Variants

<

SYNC MASTER=N/A

SYNC DATE=N/A

PAGE TITLE

K16 BOM Variants

Apple Inc.

DRAWING NUMBER

051-8467

SIZE

D

REVISION

3.3.0

BRANCH

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PAGE


5 OF 110

SHEET


5 OF 74

	8	7	6	5	4	3	2	1
D	<div>Revision History</div> <div>Proto 0 (ECO #0000876215, v1.0.0, P4 change #210266, 03/16/2010)</div> <div><div>v1.1.0 (P4 change #211399, 03/24/2010)</div><div>MCP: 7742015 - Added RC to DDC pass FETs to avoid glitch (pp. 7, 93). 7788138 - Added feedback divider and BOM tables for more HVDD LDOs (pp. 4, 25). SMC: 7761747 - Added resistors to connect TCON to SMC or MCP SMBus (pp. 4, 52, 90). 7787883 - Added support for DP HPD wake / S4 state (pp. 4, 7, 8, 19, 49, 50, 78, 94). SMS: 7765466 - Added S3 pull-up to SMS_INT_L to prevent leakage path (pp. 50, 59). 7769139 - Unstuffed SMS circuit (pg. 4). General: 7787897 - Property/page fixes to reduce CheckPlus warnings/errors (pp. 7, 8, 12, 17, 74, 93, 108).</div><div>v1.2.0 (P4 change #211839, 03/26/2010)</div><div>USB: 7796626 - Changed port switch from TPS2052B to TPS2069 (pg. 46). SMC: 7787883 - Added PLACE_NEAR property on R5022 to avoid stub (pg. 50). SMBus: 7761747 - Added TCON I2C nets to FUNC_TEST list for J9000 (pg. 7). Power: 7796648 - Changed DP and LCD power from PP3V3_S3 to PP3V3_S5 (pp. 8, 90). 7796658 - Changed backlight driver to E00 version (pg. 97). BOM: 7796661 - Set up primary & alternate for power supply FET (pp. 4, 72). 7796654 - Consolidated SSM6N15FE to SSM6N37FE (pg. 48). 7796658 - Changed RCs on some SMC analog inputs (pg. 54). 7796683 - Stuffed RC on backlight driver PWM input (pg. 97). General: 7796631 - Sorted BOM variants for easier verification (pg. 5). 7796631 - Cosmetic clean-up (pg. 76).</div><div>v1.3.0 (P4 change #212050, 03/26/2010)</div><div>SMBus: 7761747 - Added isolation FET and unstuffed series R's on TCON I2C for now (pp. 4, 90, 108). Power Supply: 7796661 - Removed alternate FET, made some FETs primary to other APN (pp. 4, 72, 73, 76). 7798425 - R/C value changes for 3.42V G3Hot power supply (pg. 69). 7798399 - R/C value changes for 5V/3.3V power supply (pg. 72). 7800179 - R value changes for CPU VCore power supply (pg. 74). 7798445 - R value changes for 0.9V S5 power supply (pg. 77). 7796658 - Changed backlight driver back to non-E00 version (pp. 4, 97). BOM: 7796658 - Added alternates for two caps per GSM and removed unused alternates (pg. 4). 7798399 - Consolidated 100pF caps (pp. 74, 75).</div><div>v1.4.0 (P4 change #212757, 03/31/2010)</div><div>MCP SPI: 7809733 - Changed strapping to select 62.5MHz SPI bus frequency (pg. 4). SMBus: 7796631 - Added XDP connection to SMBus aliases page (pp. 13, 52). 7808530 - Changed SMC 'MGMT' SMBus pull-ups from 4.7K to 2K (pg. 52). 7761747 - Documented SMBus addresses for panel (pg. 52). SD Card: 7800415 - Changed SD Card discharge R to more standard value (pg. 48). Power Supplies: 7803283 - Changed 5V S3 regulator output from 5.02V to 5.12V nominal (pg. 72). 7809760 - Stuffed C9799 and clarified tables/BOMOPTIONS around these parts (pg. 97).</div></div> <div>Proto 1 (ECO #0000884508, v2.0.0, P4 change #212783, 03/31/2010)</div> <div><div>v2.1.0 (P4 change #??????, ??/??/2010)</div><div>BOM: 7796658 - Changed OMITs to OMIT_TABLEs (pp. 10-11, 14-20, 26, 31-36, 49, 61).</div></div>							
C								
B								
A								

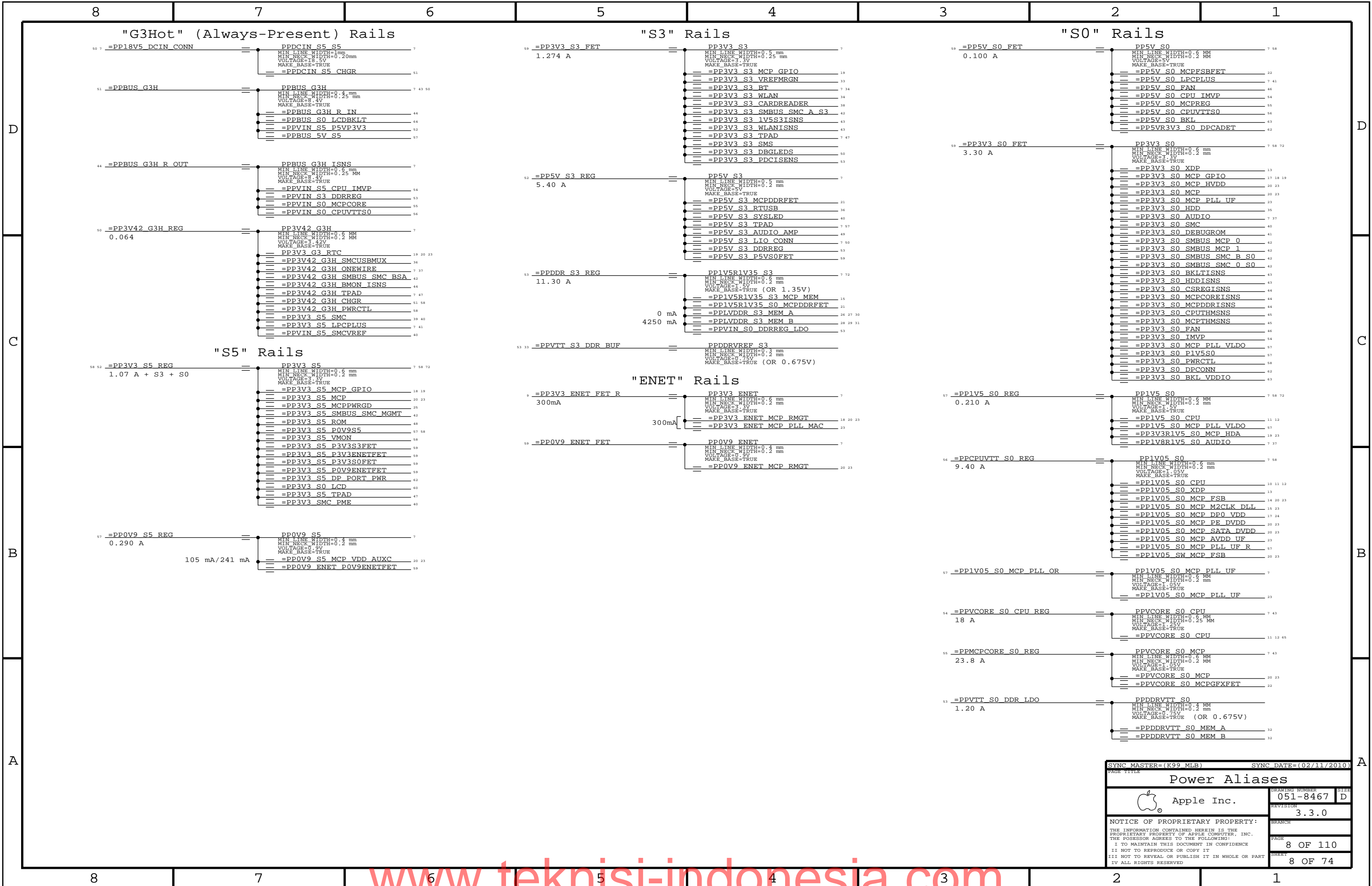
NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
Revision History			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	6 OF 110
		SHEET	6 OF 74

8	7	6	5	4	3	2	1
Functional Test Points				NO_TEST Nets			
J4001: AirPort / BT Connector				FSB Signals (Covered via CPU/MCP JTAG)			
FUNC_TEST				NO_TEST			
TRUE PP3V3 WLAN_F 7 34 40 (Need 5 TPs)				TRUE FSB A L<35..3> 10 14 66			
TRUE WIFI_EVENT_L 34 39 40				TRUE FSB ADS_L 10 14 66			
TRUE PCIE AP R2D_N 34 68				TRUE FSB ADSTB L<1..0> 10 14 66			
TRUE PCIE AP R2D_P 34 68				TRUE FSB D L<63..0> 10 14 66			
TRUE PCIE CLK100M AP_N 16 34 68				TRUE FSB DINV L<3..0> 10 14 66			
TRUE PCIE CLK100M AP_P 16 34 68				TRUE FSB DSTB L N<3..0> 10 14 66			
TRUE USB_BT_P 18 34 69				TRUE FSB DSTB L P<3..0> 10 14 66			
TRUE USB_BT_N 18 34 69				TRUE FSB HIT_L 10 14 66			
TRUE PCIE AP D2R_P 16 34 68				TRUE FSB HITM_L 10 14 66			
TRUE PCIE AP D2R_N 16 34 68				TRUE FSB LOCK_L 10 14 66			
TRUE PCIE_WAKE_L 16 34				TRUE FSB REQ L<4..0> 10 14 66			
TRUE AP_RESET_CONN_L 34							
TRUE AP_CLKREQ_O_L 34							
TRUE =PP3V3_S3_BT 8 34							
(Need to add 6 GND TPs)							
J4501: SATA SSD Connector							
FUNC_TEST							
TRUE PP3V3_S0_HDD_R 7 35 (Need 5 TPs)							
TRUE SATA_HDD_D2R_C_P 35 68							
TRUE SATA_HDD_D2R_C_N 35 68							
TRUE SATA_HDD_R2D_N 35 68							
TRUE SATA_HDD_R2D_P 35 68							
TRUE SMC_HDD_QOB_TEMP 35 39							
TRUE SMC_HDD_TEMP_CTL 35 39							
(Need to add 6 GND TPs)							
J4700: LIO Connector							
FUNC_TEST							
TRUE =PP3V42_G3H_ONEWIRE 8 37 (Need 2 TPs)							
TRUE =PP3V3_S0_AUDIO 8 37							
TRUE =PP1V8R1V5_S0_AUDIO 8 37							
TRUE SYS_ONEWIRE 37 39							
TRUE SMC_BC_ACOK 9 37 39 40							
TRUE =USB_PWR_EN 36 37 58							
TRUE SMC_LID 7 37 39 40 47							
TRUE =I2C_LIO_SDA 37 42							
TRUE =I2C_LIO_SCL 37 42							
TRUE =I2C_MIKEY_SCL 37 42							
TRUE =I2C_MIKEY_SDA 37 42							
TRUE AUD_IPHS_SWITCH_EN 19 37							
TRUE AUD_IP_PERIPHERAL_DET 17 37							
TRUE AUD_I2C_INT_L 19 37							
TRUE AUD_GPIO_3 37 48							
TRUE SPKRAMP_INR_N 37 49 72							
TRUE SPKRAMP_INR_P 37 49 72							
TRUE USB_EXTD_N 18 37 69							
TRUE USB_EXTD_P 18 37 69							
TRUE USB_CAMERA_N 18 37 69							
TRUE USB_CAMERA_P 18 37 69							
TRUE HDA_SDOUT 19 37 69							
TRUE HDA_BIT_CLK 19 37 69							
TRUE HDA_SDIN0 19 37 69							
TRUE USB_EXTD_OC_L 18 37							
TRUE HDA_RST_L 19 37 69							
TRUE HDA_SYNC 19 37 69							
(Need to add 5 GND TPs)							
J4800: SD Card Connector							
FUNC_TEST							
TRUE PP3V3_SW_SD_PWR 38							
TRUE SD_CLK 38 70							
TRUE SD_CMD 38 70							
TRUE SD_D<7..0> 38 70							
TRUE SD_CD_L 38							
TRUE SD_WP 38							
(Need to add 2 GND TPs)							
J5100: LPC+SPI Connector							
FUNC_TEST							
TRUE =PP3V3_S5_LPCPLUS 8 41							
TRUE =PP5V_S0_LPCPLUS 8 41							
TRUE LPC_AD<3..0> 19 39 41 69							
TRUE SPI_ALT_MOSI 41 69							
TRUE SPI_ALT_MISO 41 69							
TRUE LPC_FRAME_L 19 39 41 69							
TRUE PM_CLKRUN_L 19 39 41							
TRUE SMC_TMS 39 40 41							
TRUE LPCPLUS_RESET_L 25 41							
TRUE SMC_TDO 39 40 41							
TRUE SMC_TRST_L 39 41							
TRUE SMC_MD1 39 41							
TRUE SMC_TX_L 36 39 40 41							
TRUE LPC_CLK33M_LPCPLUS 25 41 69							
TRUE SPIROM_USE_MLB 19 41 48							
TRUE SPI_ALT_CLK 41 69							
TRUE SPI_ALT_CS_L 41 69							
TRUE LPC_SERIRQ 19 39 41							
TRUE LPC_PWRDWN_L 19 39 41							
TRUE SMC_TDI 39 40 41							
TRUE SMC_TCK 39 40 41							
TRUE SMC_RESET_L 39 40 41 51							
TRUE SMC_NMI 39 41							
TRUE SMC_RX_L 36 39 40 41							
TRUE LPCPLUS_GPIO 19 41							
(Need to add 6 GND TPs)							
J5600: Fan Connector							
FUNC_TEST							
TRUE PP5V_S0 7 8 58							
TRUE FAN_RT_TACH 46							
TRUE FAN_RT_PWM 46							
(Need to add 1 GND TP)							
J5700: IPD Flex Connector							
FUNC_TEST							
TRUE =PP5V_S3_TPAD 8 57							
TRUE =PP3V42_G3H_TPAD 8 47							
TRUE =PP3V3_S3_TPAD 8 47							
TRUE USB_TPAD_CONN_P 47 72							
TRUE USB_TPAD_CONN_N 47 72							
TRUE =I2C_TPAD_SDA 42 47							
TRUE =I2C_TPAD_SCL 42 47							
TRUE SMC_ONOFF_L 39 40 47							
TRUE SMC_LID 7 37 39 40 47							
TRUE SMC_TPAD_RST_L 40 47							
(Need to add 5 GND TPs)							
J6900: DC-In Connector							
FUNC_TEST							
TRUE =PP18V5_DCIN_CONN 8 50 (Need 6 TPs)							
TRUE =PP5V_S3_LIO_CONN 8 50							
(Need to add 6 GND TPs)							
J6903: Speaker Connector							
FUNC_TEST							
TRUE SPKRAMP_R_P_OUT 49 50							
TRUE SPKRAMP_R_N_OUT 49 50							
J6950: Battery Connector							
FUNC_TEST							
TRUE PPVBAT_G3H_CONN 50 51 (Need 4 TPs)							
TRUE SMBUS_SMC_BSA_SCL 42 71							
TRUE SMBUS_SMC_BSA_SDA 42 71							
TRUE SYS_DETECT_L 50							
(Need to add 4 GND TPs near J6950 and 1 for shield)							
J9000: Internal DP Connector							
FUNC_TEST							
TRUE PPVOUT_SW_LCDBKLT 7 41 60 63 (Need 2 TPs)							
TRUE PP3V3_SW_LCD 60 (Need 2 TPs)							
TRUE =I2C_TCON_SDA 42 60							
TRUE LED_RETURN_6 40 63							
TRUE LED_RETURN_5 60 63							
TRUE LED_RETURN_4 60 63							
TRUE LED_RETURN_3 60 63							
TRUE LED_RETURN_2 60 63							
TRUE LED_RETURN_1 60 63							
TRUE DP_INT_HPD_CONN 60							
TRUE DP_INT_AUX_CH_C_N 60 72							
TRUE DP_INT_AUX_CH_C_P 60 72							
TRUE DP_INT_ML_F_P<0> 60 72							
TRUE DP_INT_ML_F_N<0> 60 72							
TRUE DP_INT_ML_F_P<1> 60 72							
TRUE DP_INT_ML_F_N<1> 60 72							
TRUE =I2C_TCON_SCL 42 60							
(Need to add 5 GND TPs)							
Misc Voltages & Control Signals							
FUNC_TEST							
TRUE PPVOUT_SW_LCDBKLT 7 41 60 63							
TRUE PPDCIN_S5_S5 8							
TRUE PPBUS_G3H 8 41 50							
TRUE PPBUS_G3H_ISNS 8							
TRUE PP5V_S3 8							
TRUE PP5V_S3_RTUSB_A_F 16							
TRUE PP5V_S0 7 8 58							
TRUE PP3V42_G3H 8							
TRUE PP3V3_S5 8 58 72							
TRUE PP3V3_SW_DPPWR 62							
TRUE PP3V3_S3 8							
TRUE PP3V3_WLAN_F 7 34 40							
TRUE PP3V3_S0 8 58 72							
TRUE PP3V3_S0_HDD_R 7 35							
TRUE PP3V3_ENET 8							
TRUE PP1V5R1V35_S3 8 72							
TRUE PP1V5_S0 8 58 72							
TRUE PP1V05_S0 8 58							
TRUE PP1V05_S0_MCP_PLL_UF 8							
TRUE PP0V9_S5 8							
TRUE PP0V9_ENET 8							
TRUE PPVCORE_S0_CPU 8 41							
TRUE PPVCORE_S0_MCP 8 41							
(Need to add 27 GND TPs)							
TRUE SMC_PM_G2_EN 39 58							
TRUE PM_SLP_S4_L 19 39 58							
TRUE PM_SLP_S3_L 19 39 40 58							

SYNC MASTER=(K99 MLB)		SYNC DATE=(02/16/2010)	
PAGE TITLE			
Functional Test / No Test			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		7 OF 110	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		7 OF 74	
IV ALL RIGHTS RESERVED			

www.teknisi-indonesia.com




SYNC MASTER=(K99 MLB)

SYNC DATE=(02/11/2010)

PAGE TITLE

Power Aliases

 Apple Inc.

DRAWING NUMBER
051-8467

SIZE
D

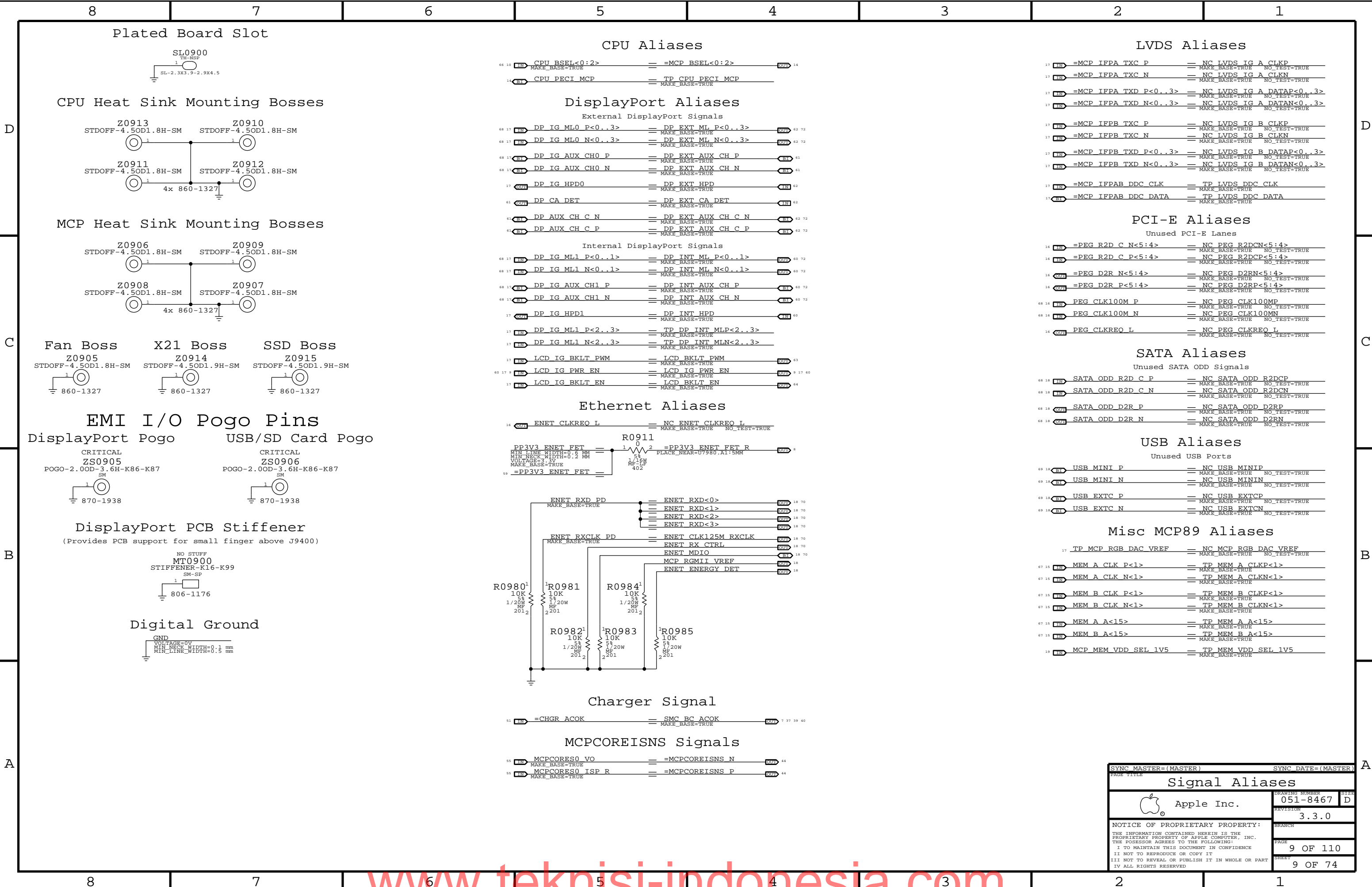
REVISION
3.3.0

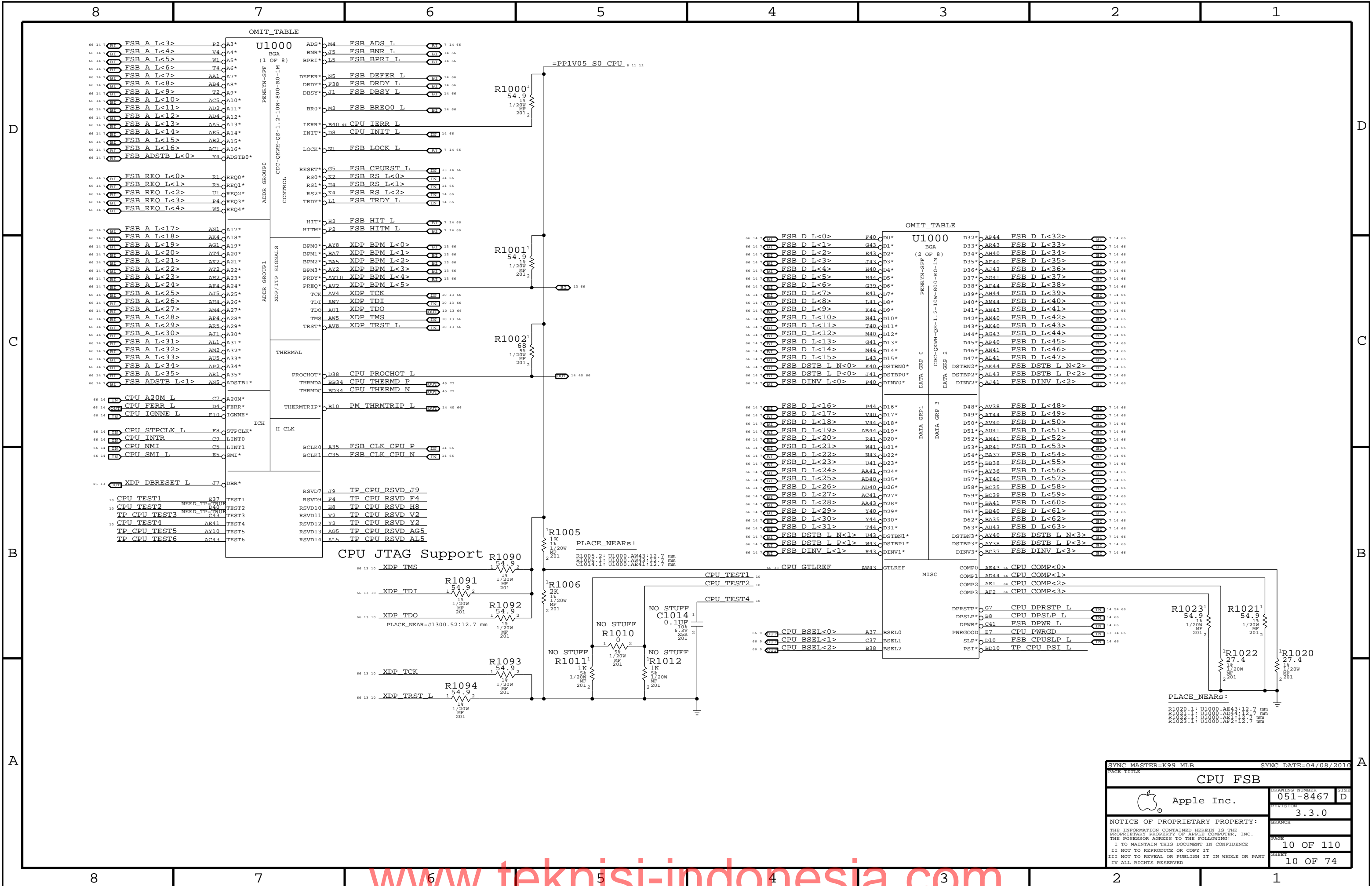
BRANCH

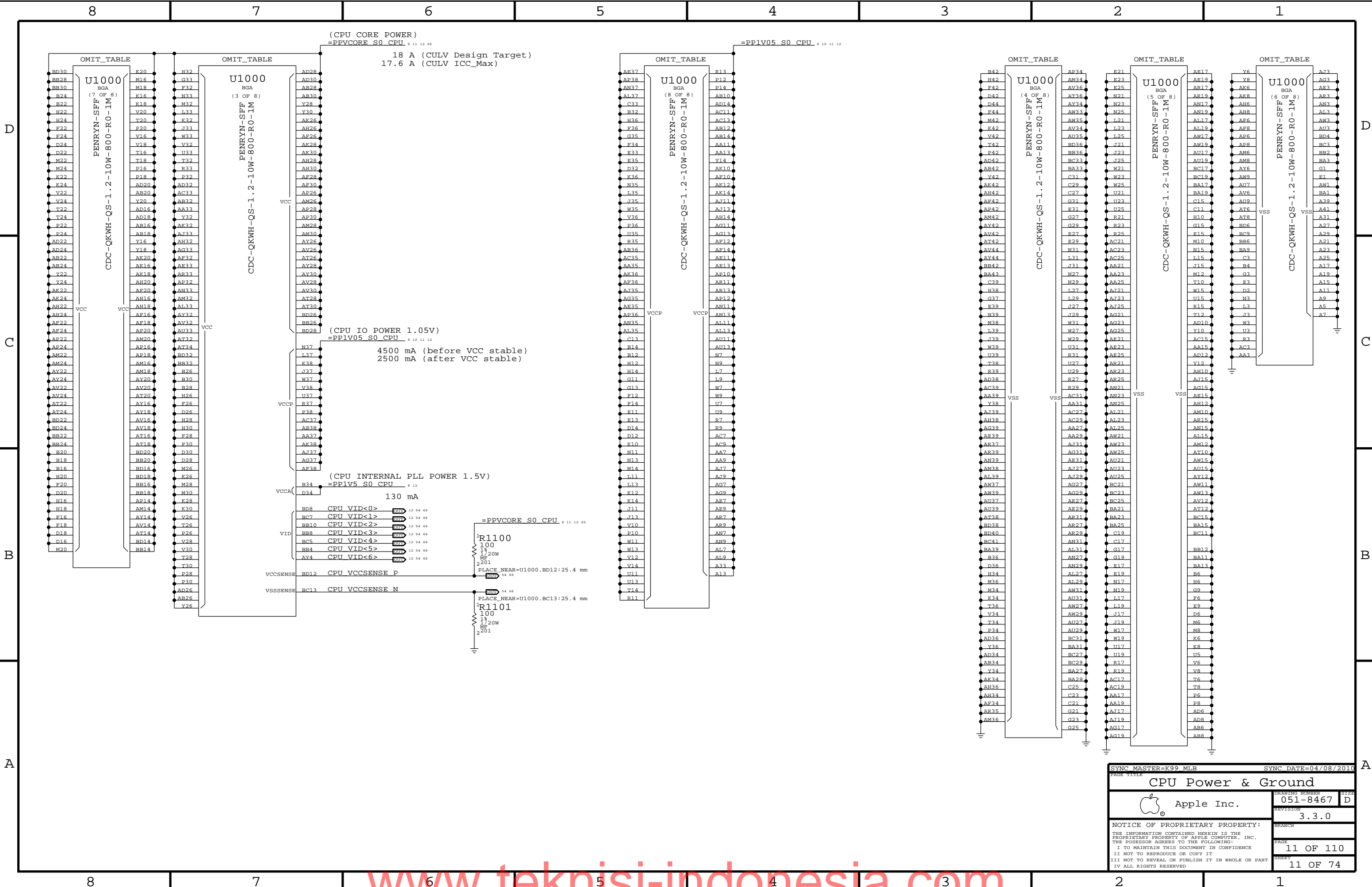
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PAGE
8 OF 110

SHEET
8 OF 74







4x 270uF. 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

[illegible][illegible][illegible]

CRITICAL
OMIT TABLE
1 C1230
10UF
20%
6.3V
X5R
603

CRITICAL
NO STUFF
1 C1231
10UF
20%
6.3V
X5R
603

[illegible][illegible][illegible]

```
66 54 11  IN CPU_VID<0..6> = IMVP6_VID<0..6> OUT 66
          MAKE_BASE=TRUE
```

11 8 =PP1V5_S0_CPU 1x 10uF, 1x 0.01uF

OMIT_TABLE
C1280
10uF
20V
6
25V
25R
503

1
2

C1281
0.01uF
13V
25R
201


LAYOUT NOTE:
PLACE C1281 NEAR PIN B34 OF U1000

11 10 8 =PP1V05 S0 CPU 1x 270uF, 12x 2.2uF

PCB layout diagram for the power plane showing decoupling capacitor placement. The diagram includes two rows of components. The top row contains six capacitors labeled C1283 through C1288, each with a value of 2.2UF, 6.3V, CERW, and 402-LF. The bottom row contains seven capacitors labeled C1290 through C1296, each with a value of 270UF, 2.2UF, 6.3V, CERW, and 402-LF. A 'CRITICAL' label is placed near C1290. A 'LAYOUT NOTE' section at the bottom provides placement instructions: C1290 close to CPU, C1283-C1288 close to FSB address pins, and C1291-C1296 close to FSB data pins. The diagram shows a power plane with a ground plane below it, and a network of decoupling capacitors connected to the power plane.

CRITICAL C1290 270UF 2.2UF 6.3V CERW 402-LF

LAYOUT NOTE:
 PLACE C1290 CLOSE TO CPU
 PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
 PLACE C1291-C1296 CLOSE TO FSB DATA PINS

SYNC MASTER=(K99 MLB)		SYNC DATE=(02/11/2010)	
PAGE TITLE			
CPU Decoupling & VID			
	Apple Inc.		DRAWING NUMBER 051-8467
			SIZE D
		REVISION 3.3.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I WILL NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED		PAGE 12 OF 110	
		SHEET 12 OF 74	


D

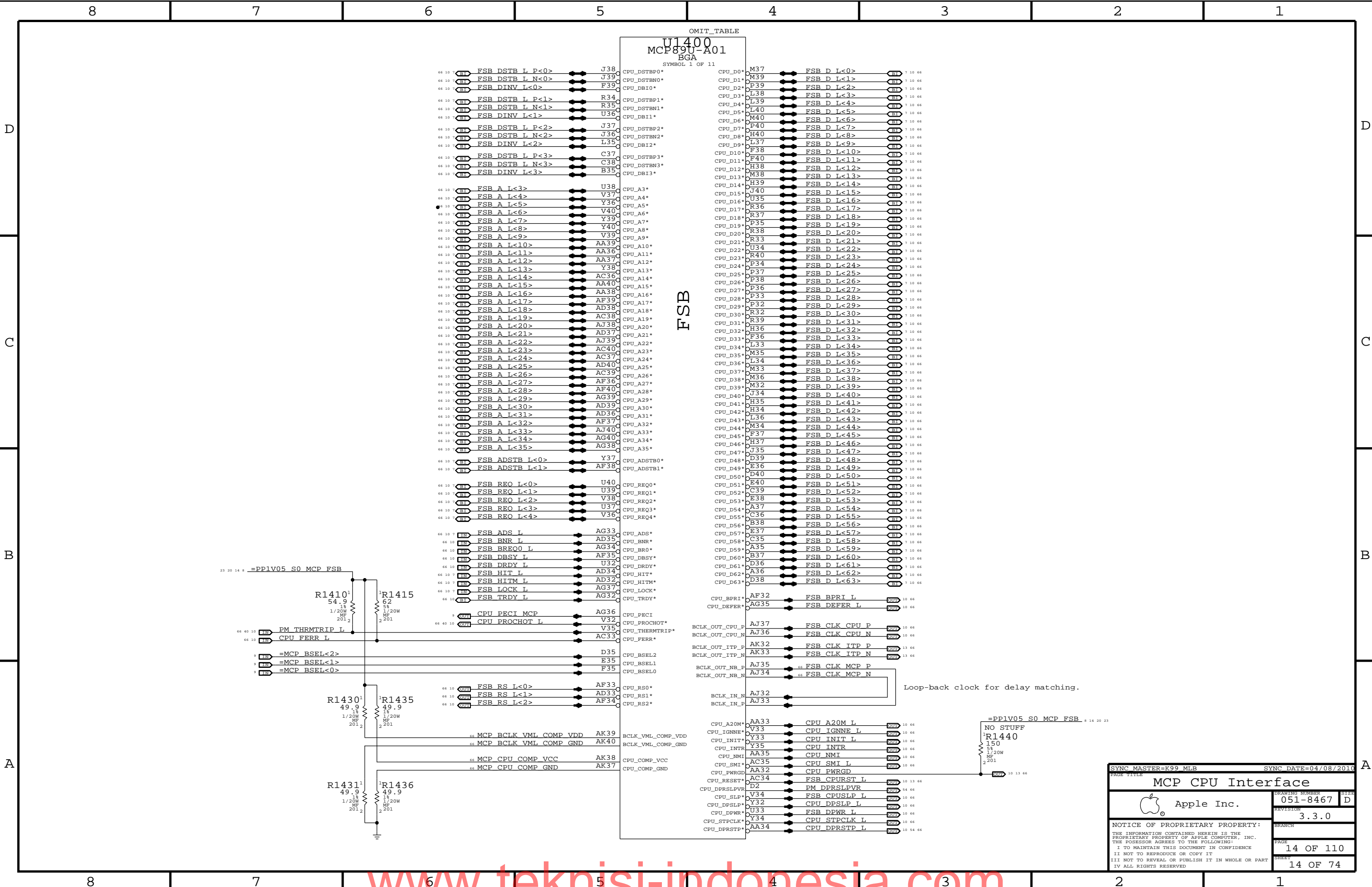
C

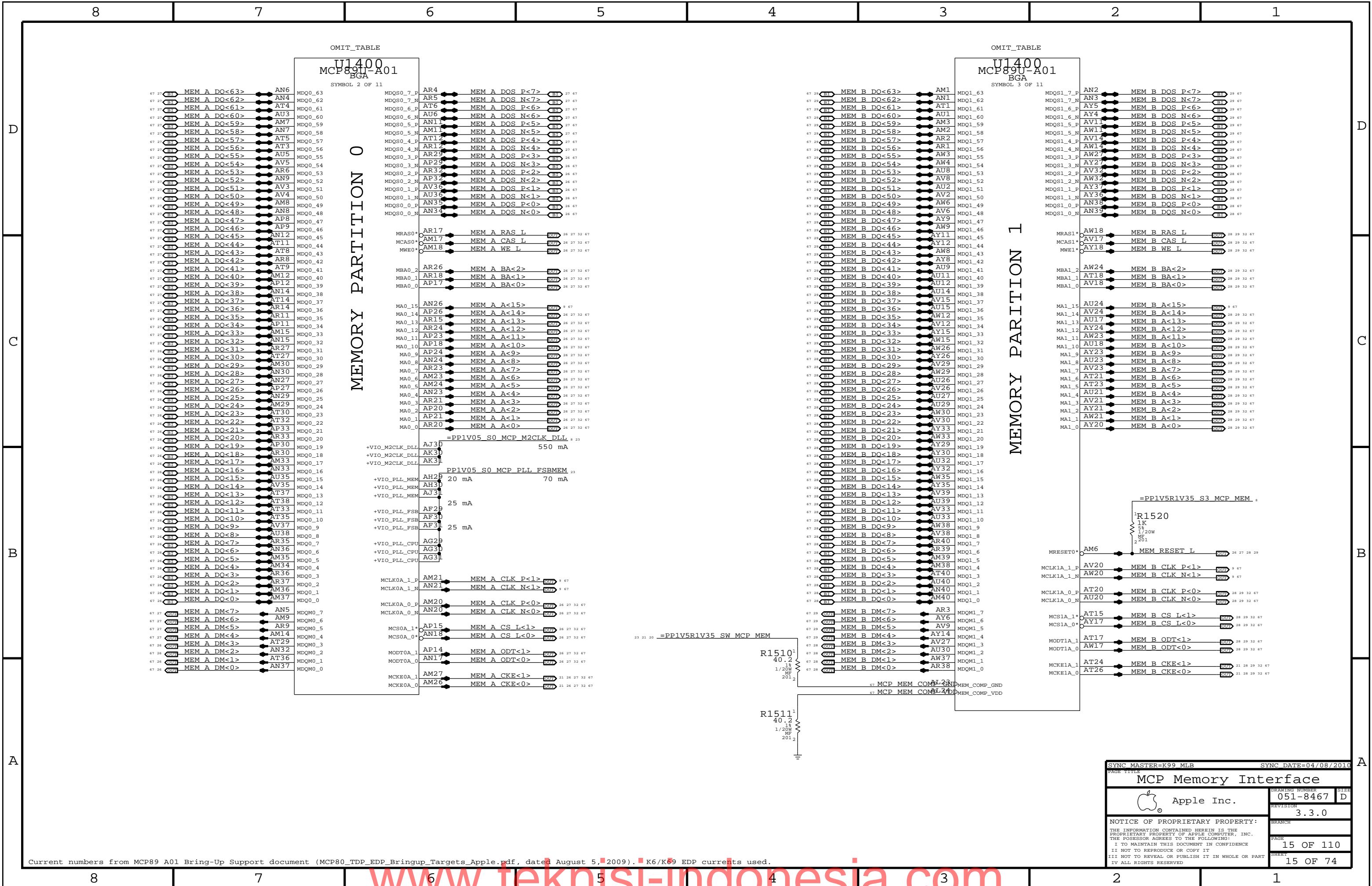
B

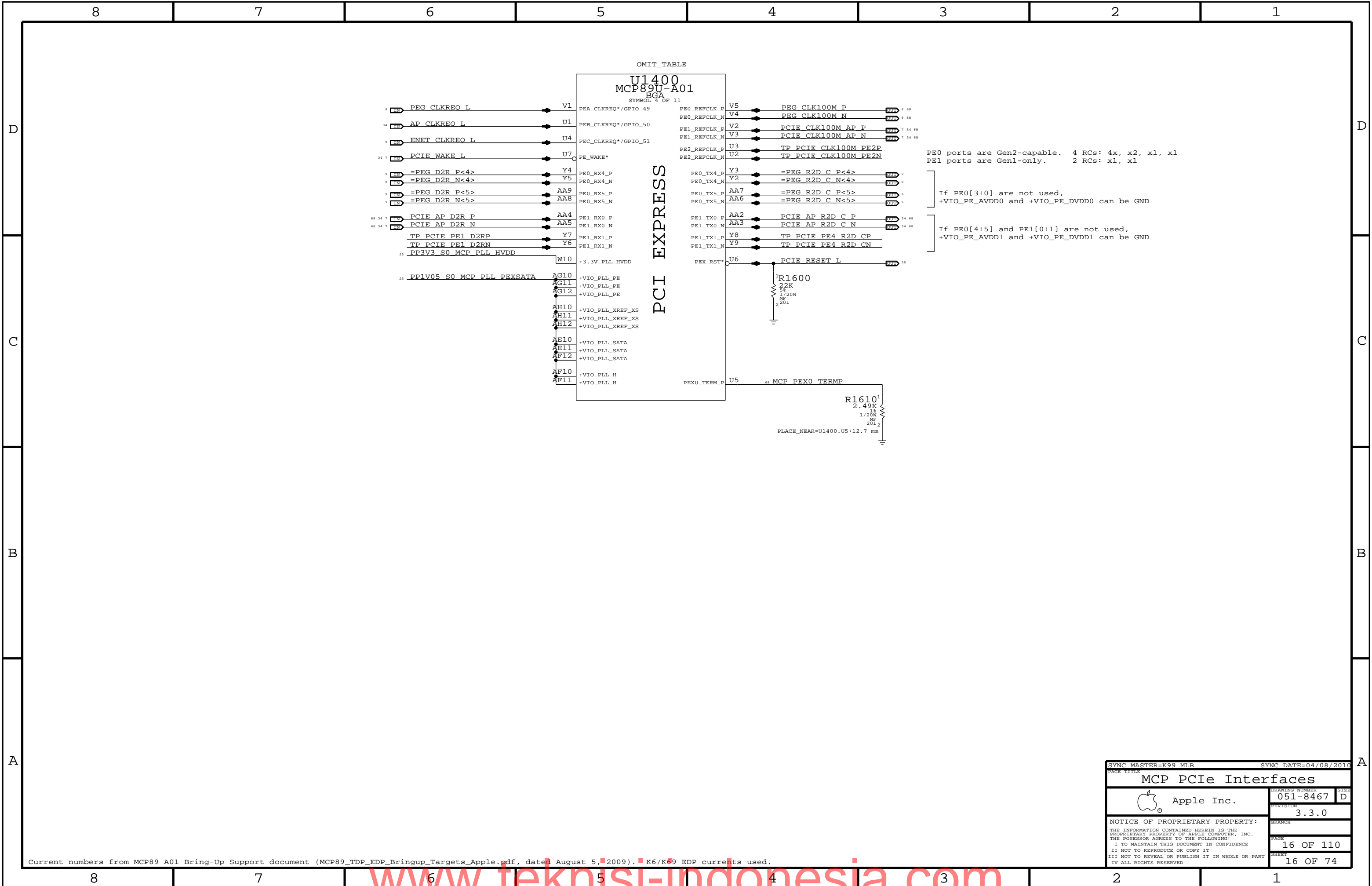


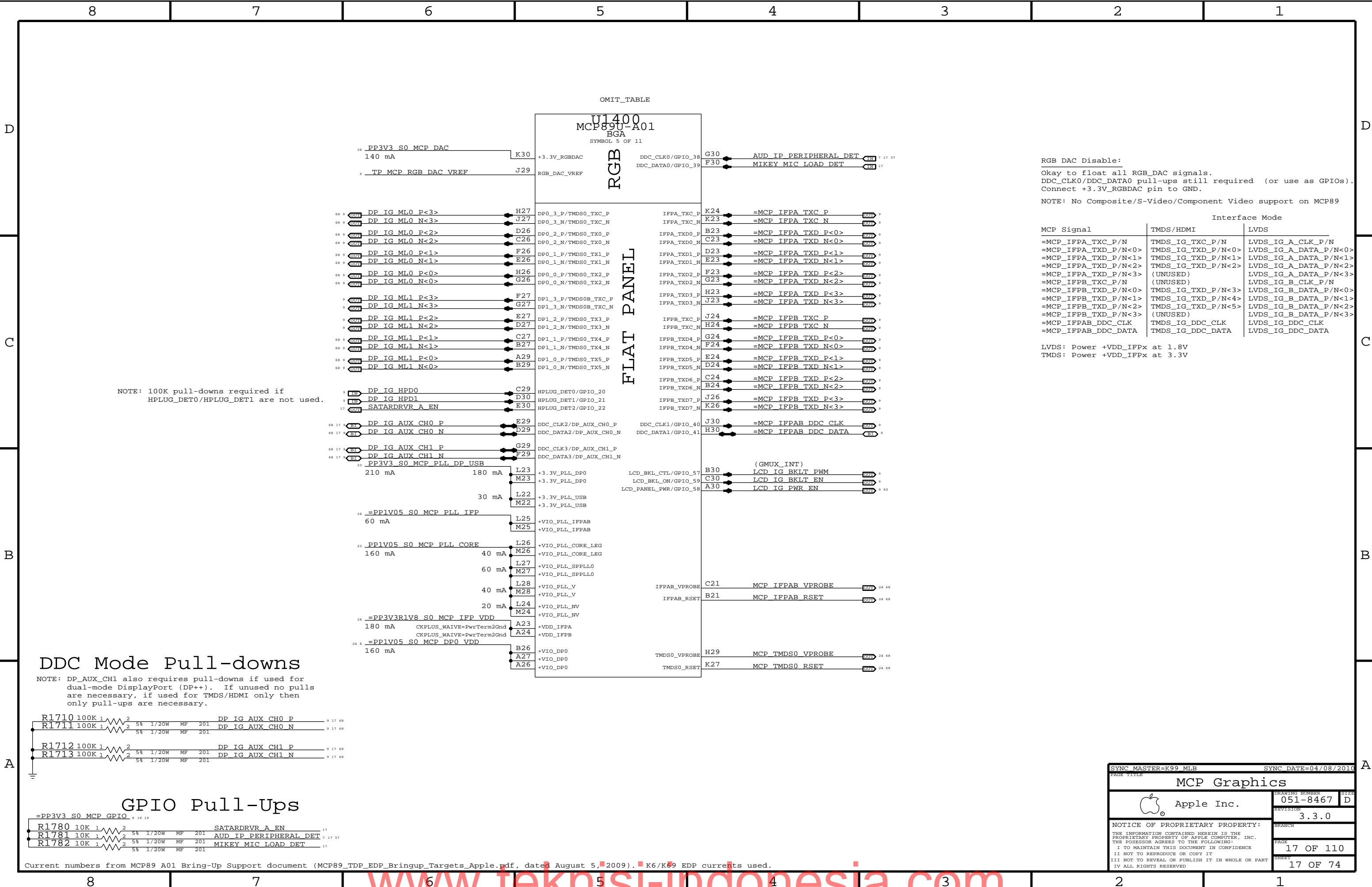
www.teknisi-indonesia.com

SYNCS MASTER=K99 MLB		SYNC DATE=03/01/2010	
PRGR TITLE		PRGR FILE	
eXtended Debug Port (Micro-XDP)			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8467		D
	REVISION		
3.3.0			
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED		13 OF 110	
		SHEET	
		13 OF 74	





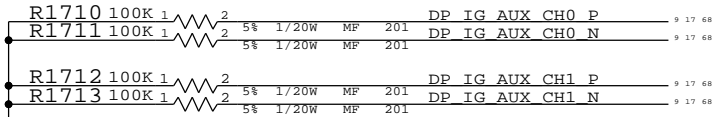




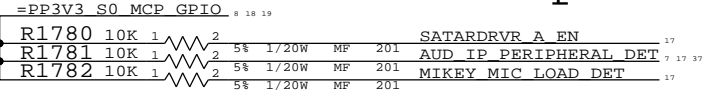
NOTE: 100K pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

DDC Mode Pull-downs

NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.



GPIO Pull-Ups



Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

RGB DAC Disable:
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
Connect +3.3V_RGBDAC pin to GND.
NOTE: No Composite/S-Video/Component Video support on MCP89

Interface Mode		
MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

LVDS: Power +VDD_IFPx at 1.8V
TMDS: Power +VDD_IFPx at 3.3V

SYNC MASTER=K99 MLB

SYNC DATE=04/08/2010

MCP Graphics

Apple Inc.

DRAWING NUMBER
051-8467

REVISION
3.3.0

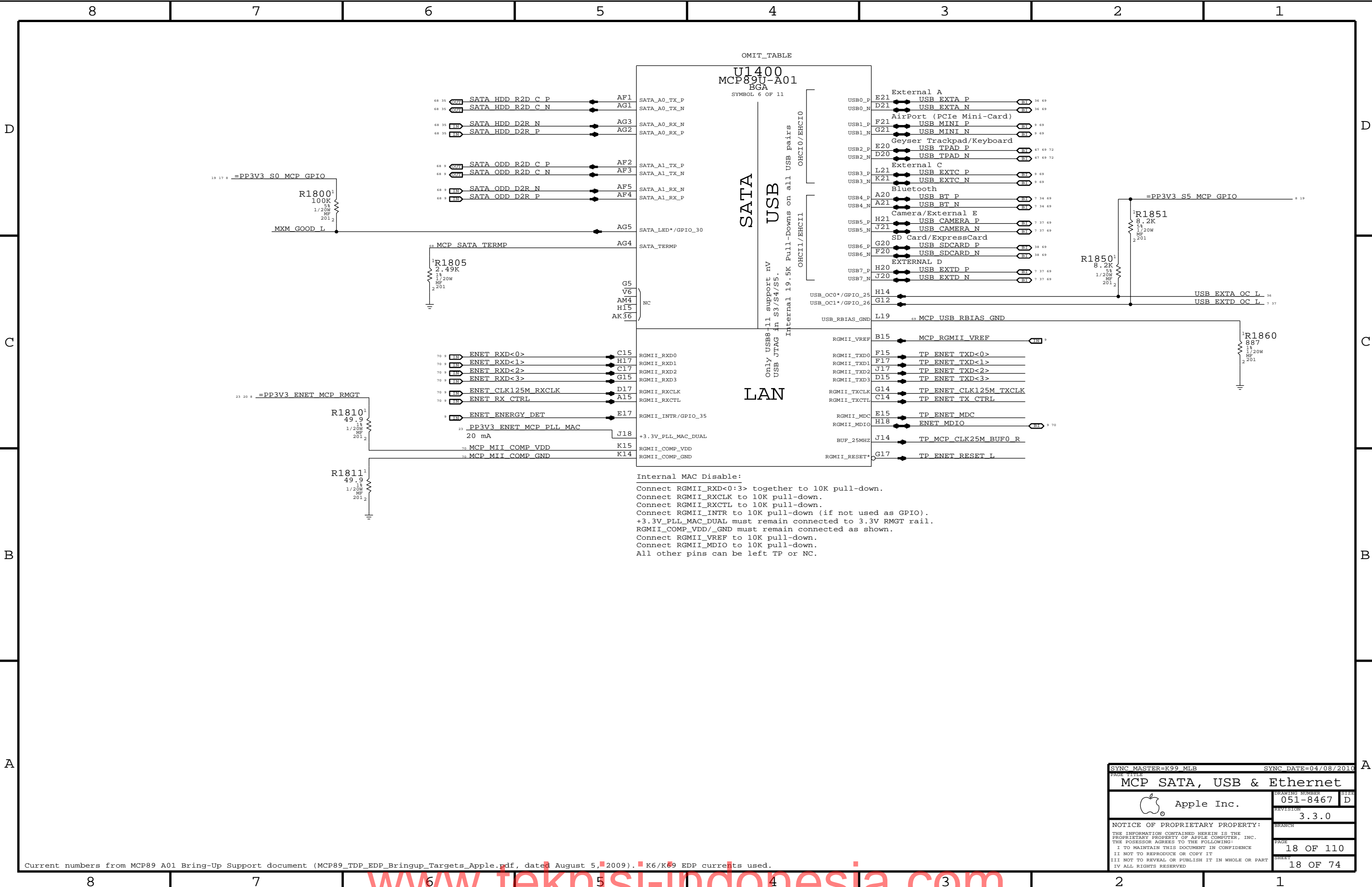
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BRANCH

PAGE
17 OF 110

SHEET
17 OF 74

www.teknisi-indonesia.com



Internal MAC Disable:
Connect RGMII_RXD<0:3> together to 10K pull-down.
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
RGMII_COMP_VDD/_GND must remain connected as shown.
Connect RGMII_VREF to 10K pull-down.
Connect RGMII_MDIO to 10K pull-down.
All other pins can be left TP or NC.

SYNC MASTER=K99 MLB

SYNC DATE=04/08/2010

MCP SATA, USB & Ethernet

Apple Inc.

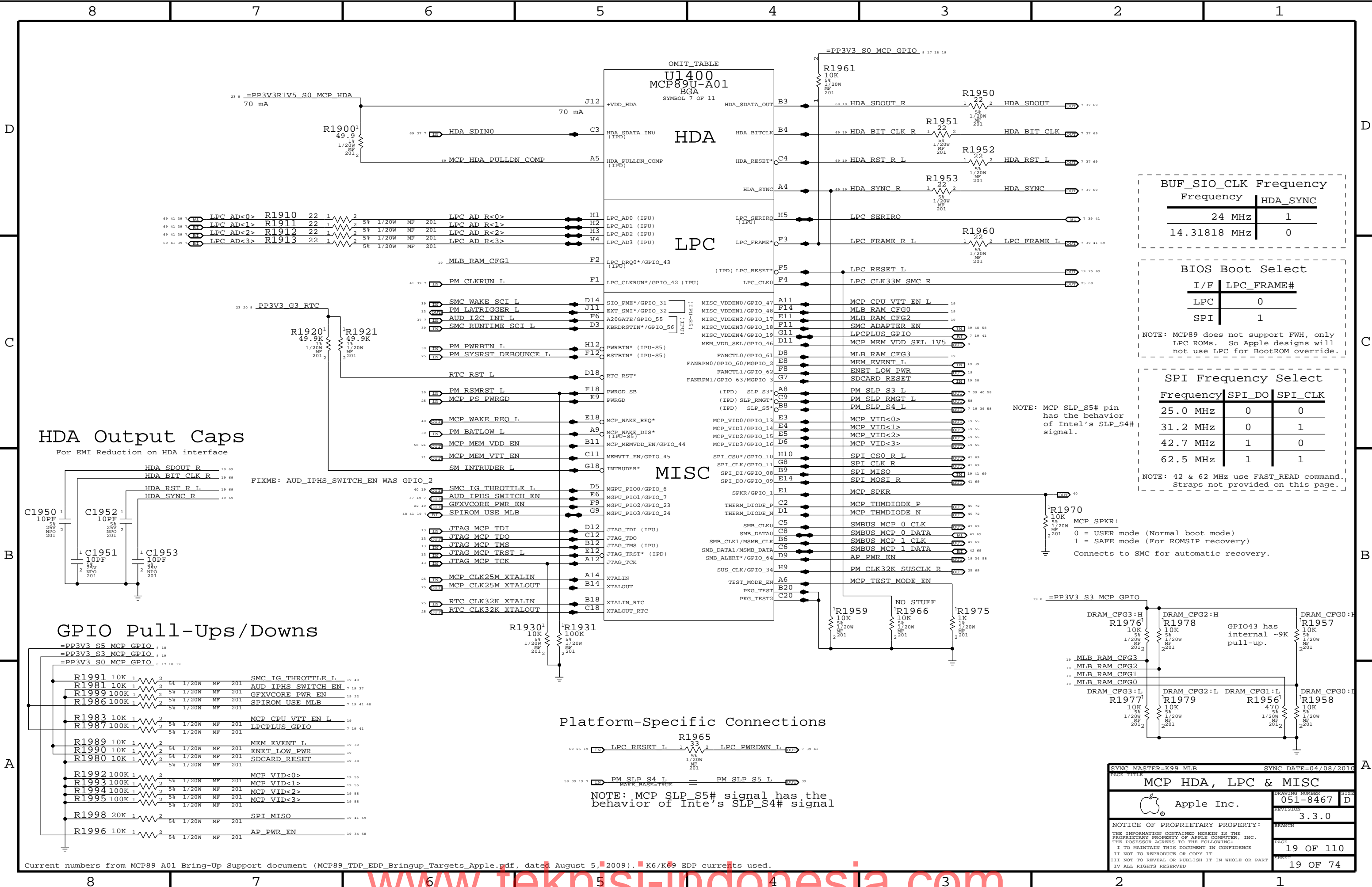
051-8467

3.3.0

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

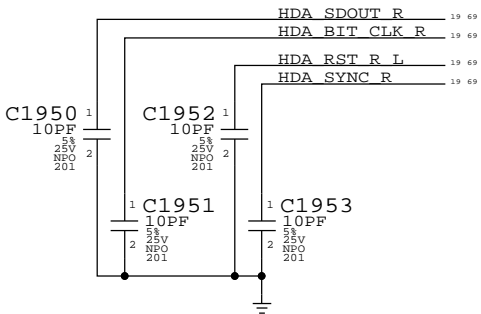
18 OF 110

18 OF 74

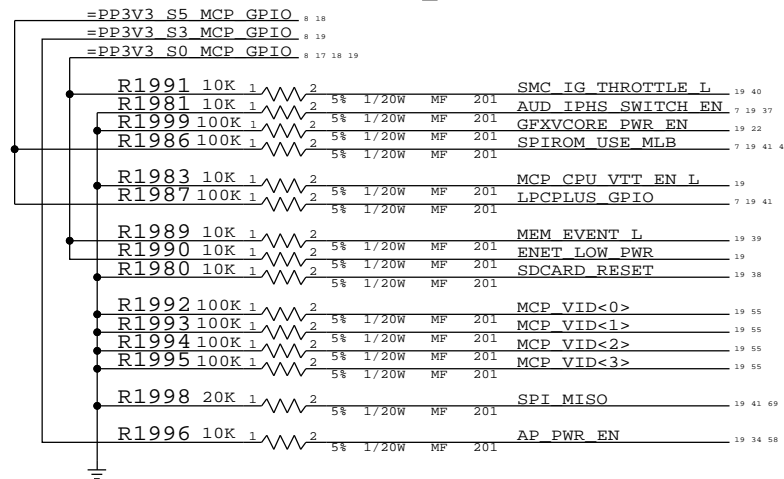


HDA Output Caps

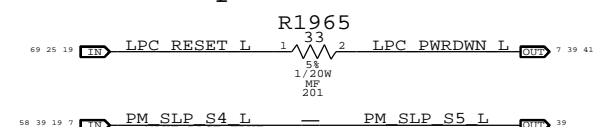
For EMI Reduction on HDA interface



GPIO Pull-Ups/Downs



Platform-Specific Connections



NOTE: MCP SLP_S5# signal has the behavior of Inte's SLP_S4# signal

BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select

I/F	LPC_FRAME#
LPC	0
SPI	1

NOTE: MCP89 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 Mhz use FAST_READ command. Straps not provided on this page.

NOTE: MCP SLP_S5# pin has the behavior of Intel's SLP_S4# signal.

MCP_SPKR:
0 = USER mode (Normal boot mode)
1 = SAFE mode (For ROMSIP recovery)
Connects to SMC for automatic recovery.

SYNC MASTER=K99 MLB

SYNC DATE=04/08/2010

MCP HDA, LPC & MISC

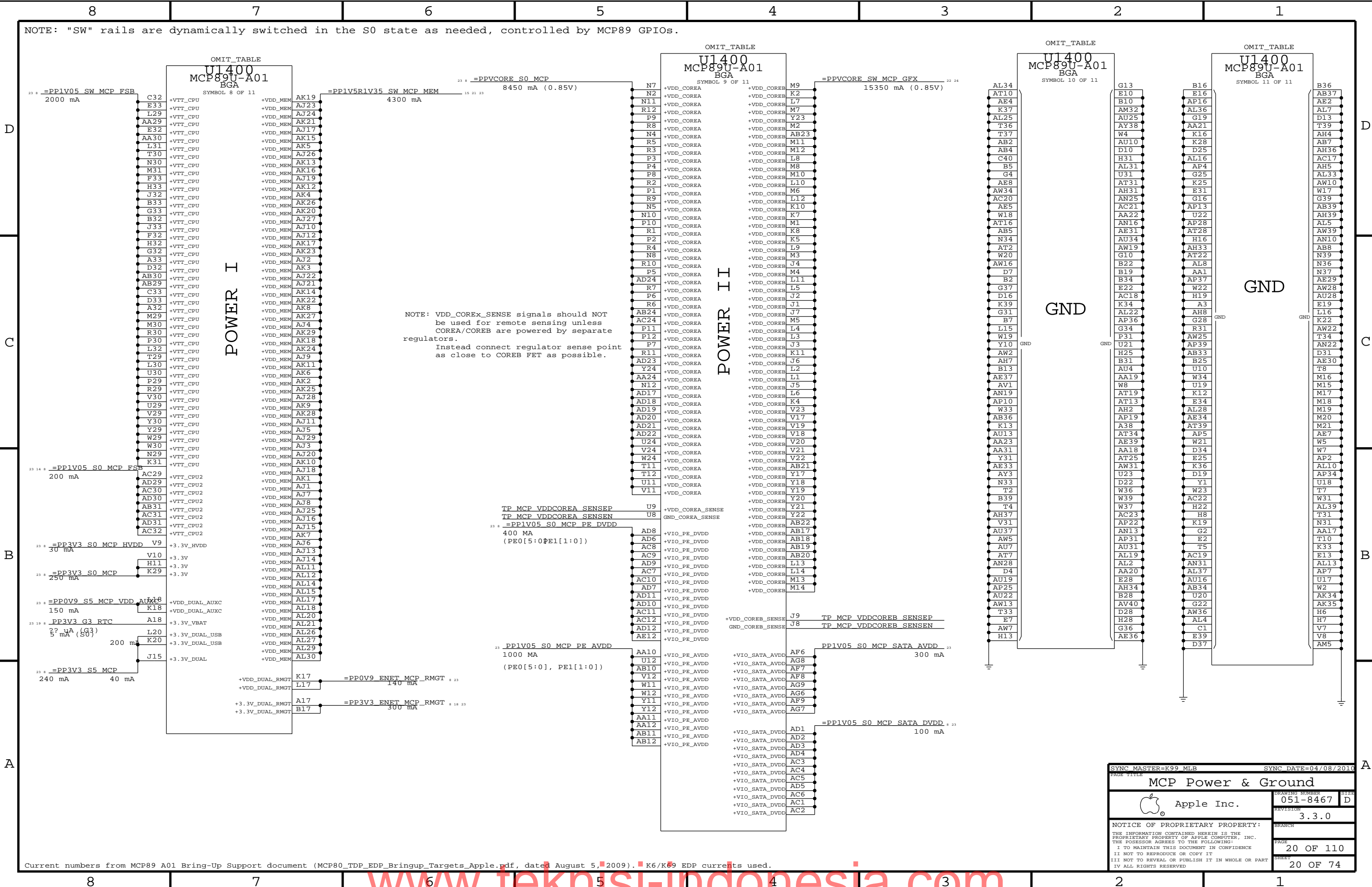
Apple Inc.

051-8467

3.3.0

19 OF 110

19 OF 74



NOTE: VDD_COREx_SENSE signals should NOT be used for remote sensing unless COREA/COREB are powered by separate regulators.
Instead connect regulator sense point as close to COREB FET as possible.

SYNC MASTER=K99 MLB

SYNC DATE=04/08/2010

MCP Power & Ground

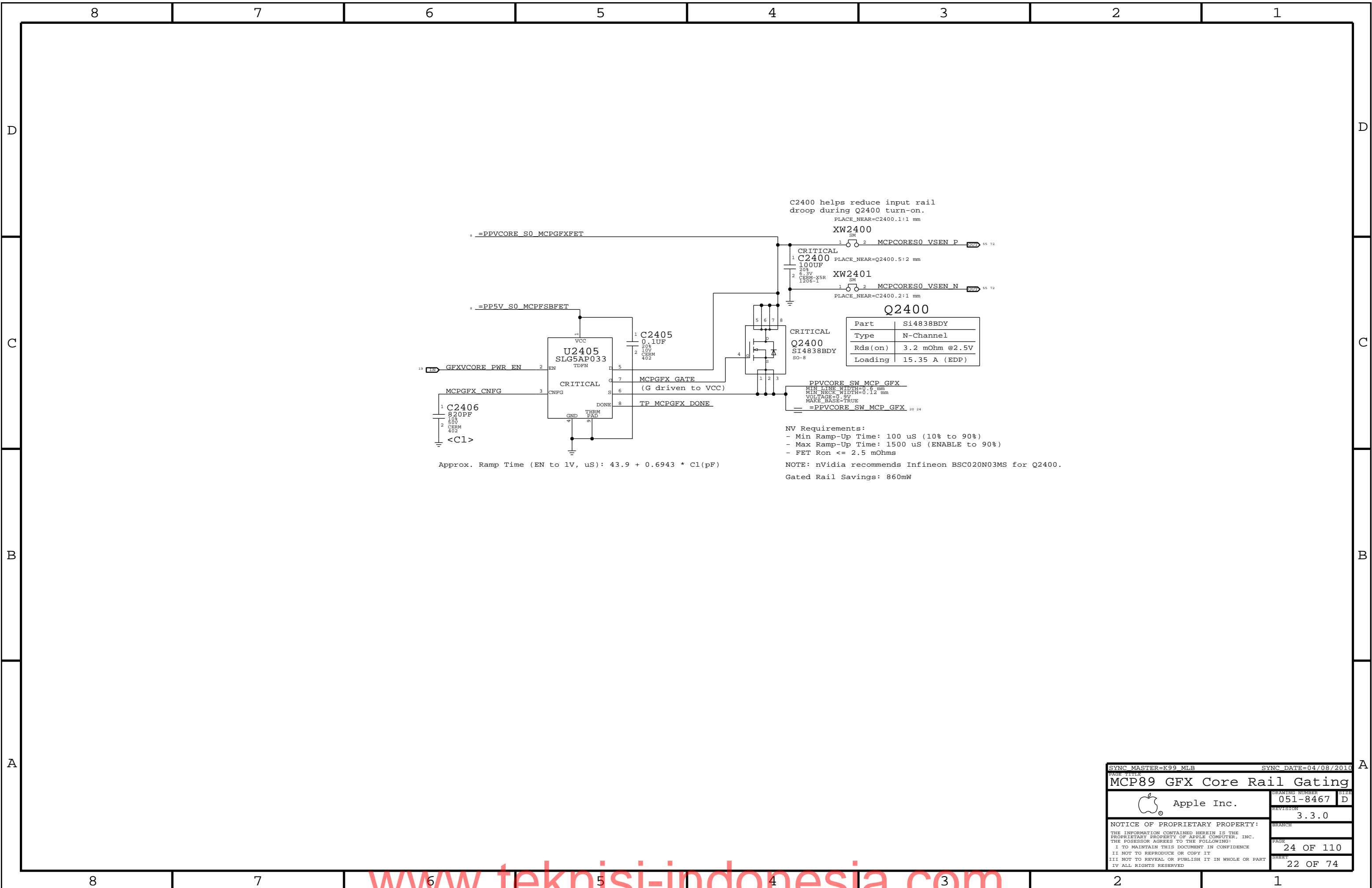
Apple Inc.

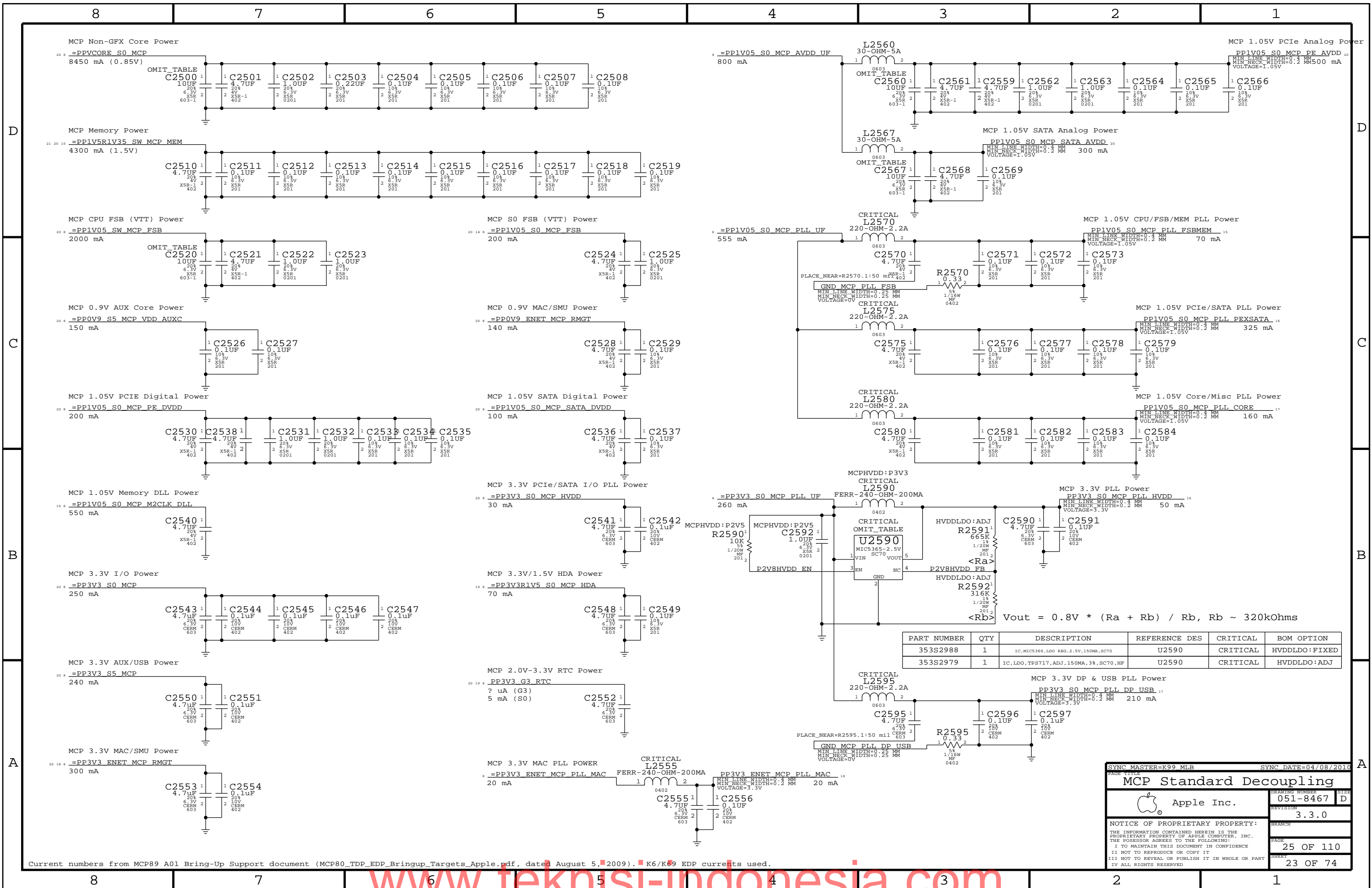
051-8467

3.3.0

20 OF 110

20 OF 74





Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2988	1	IC, MIC5366, LDO REG, 2.5V, 150mA, SC70	U2590	CRITICAL	HVDDLDO: FIXED
353S2979	1	IC, LDO, TPS717, ADJ, 150mA, 3%, SC70, HF	U2590	CRITICAL	HVDDLDO: ADJ

$$V_{out} = 0.8V * (R_a + R_b) / R_b, R_b \sim 320k\Omega$$

SYNC MASTER=K99 MLB

SYNC DATE=04/08/2010

MCP Standard Decoupling

Apple Inc.

051-8467

3.3.0

25 OF 110

23 OF 74

NOTICE OF PROPRIETARY PROPERTY:

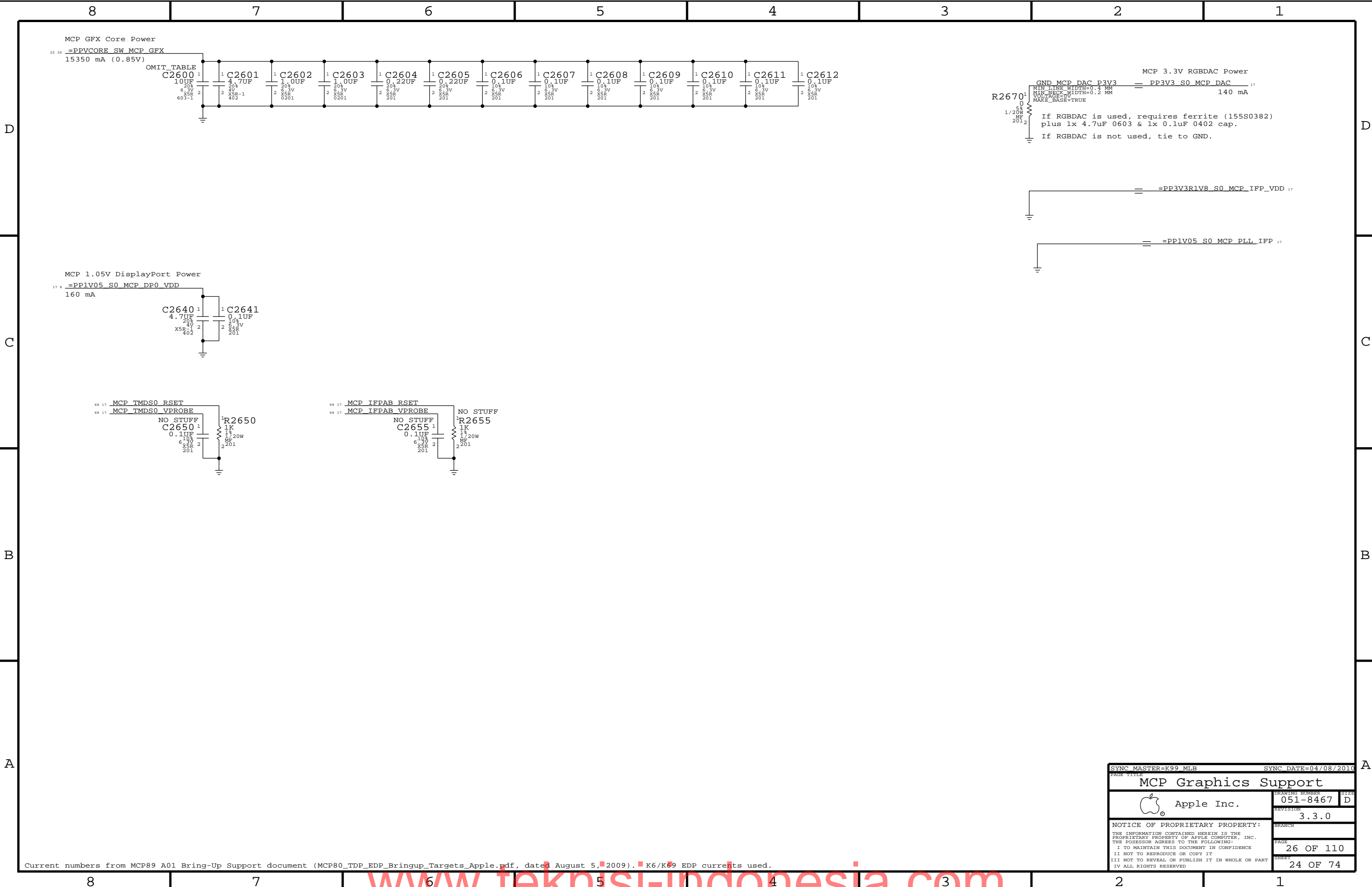
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE


II NOT TO REPRODUCE OR COPY IT

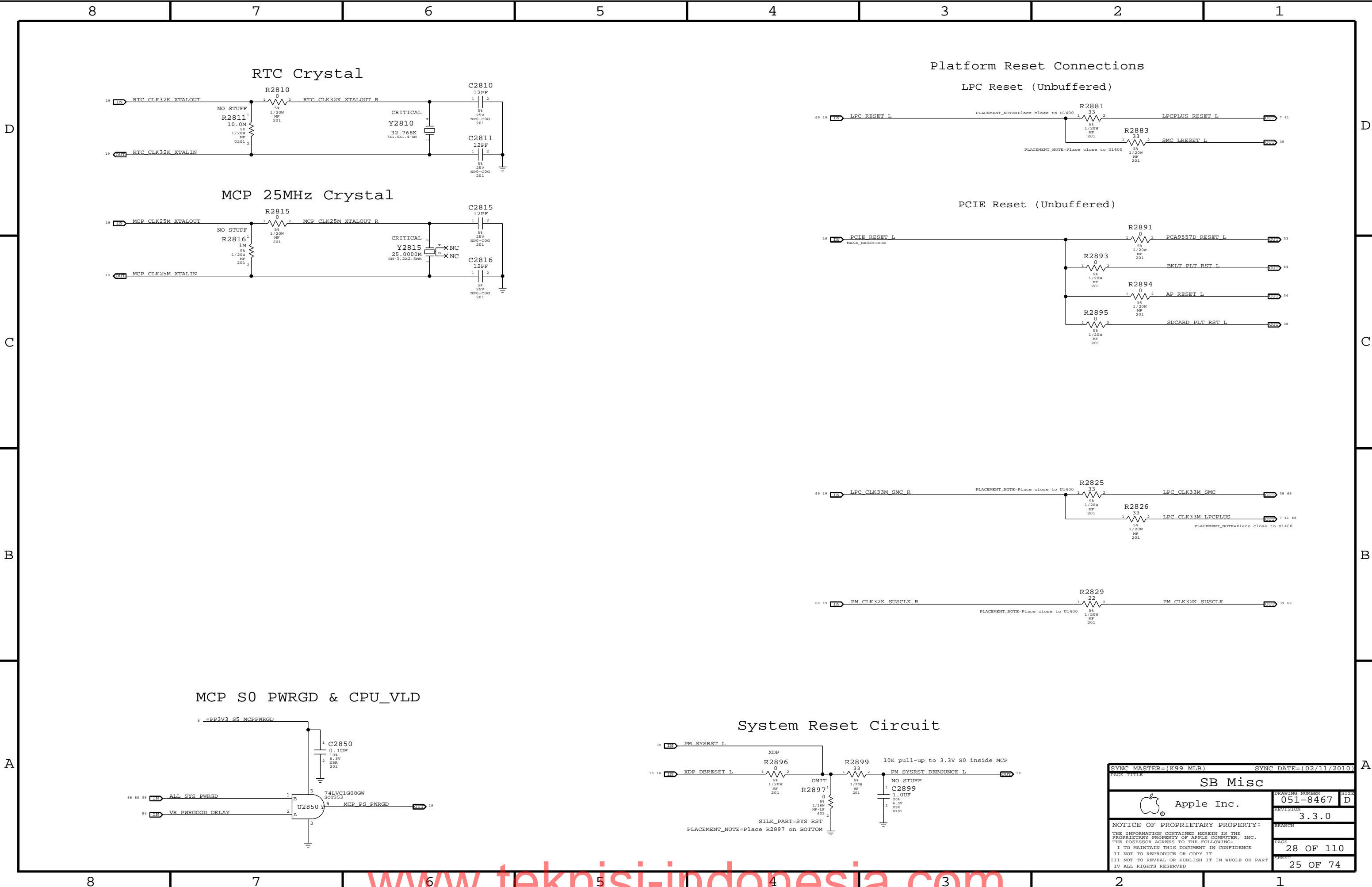
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

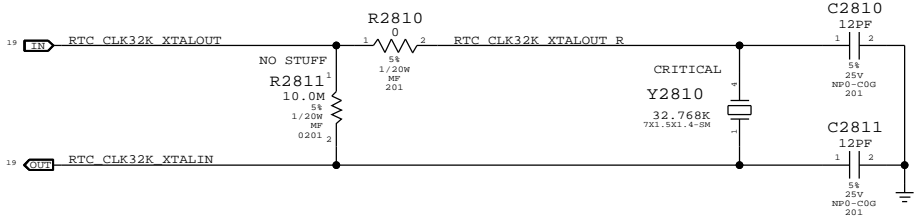


Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

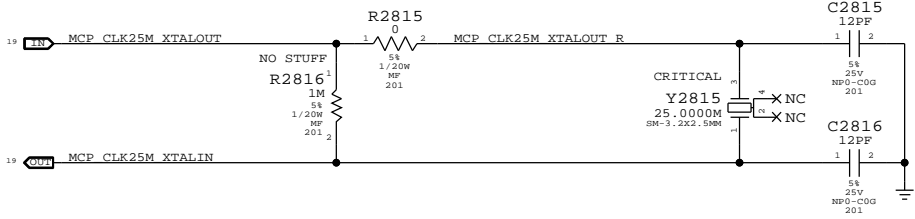
SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
MCP Graphics Support			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8467		D
	REVISION		
		3.3.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		26 OF 110	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		24 OF 74	
IV ALL RIGHTS RESERVED			



RTC Crystal

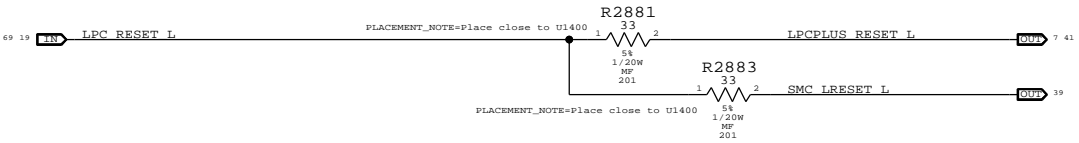


MCP 25MHz Crystal

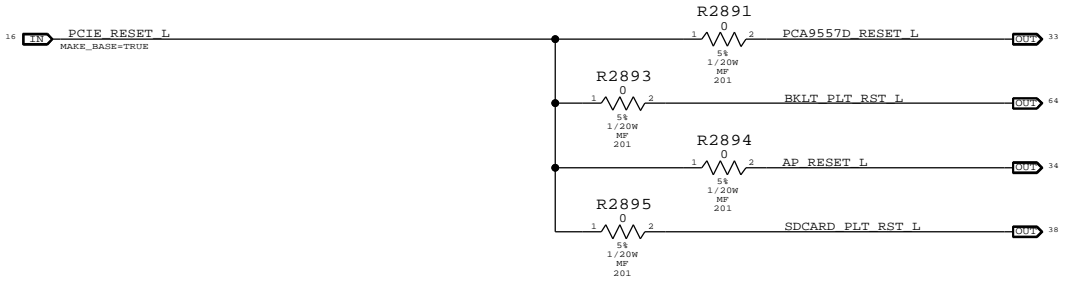


Platform Reset Connections

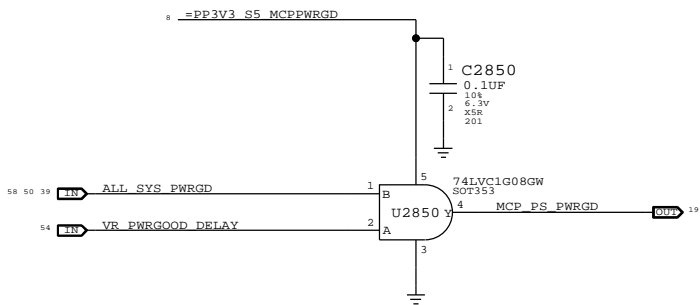
LPC Reset (Unbuffered)



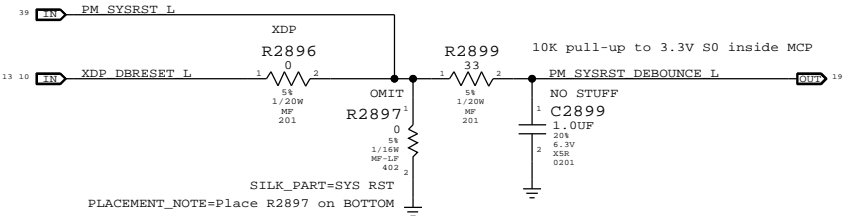
PCIE Reset (Unbuffered)




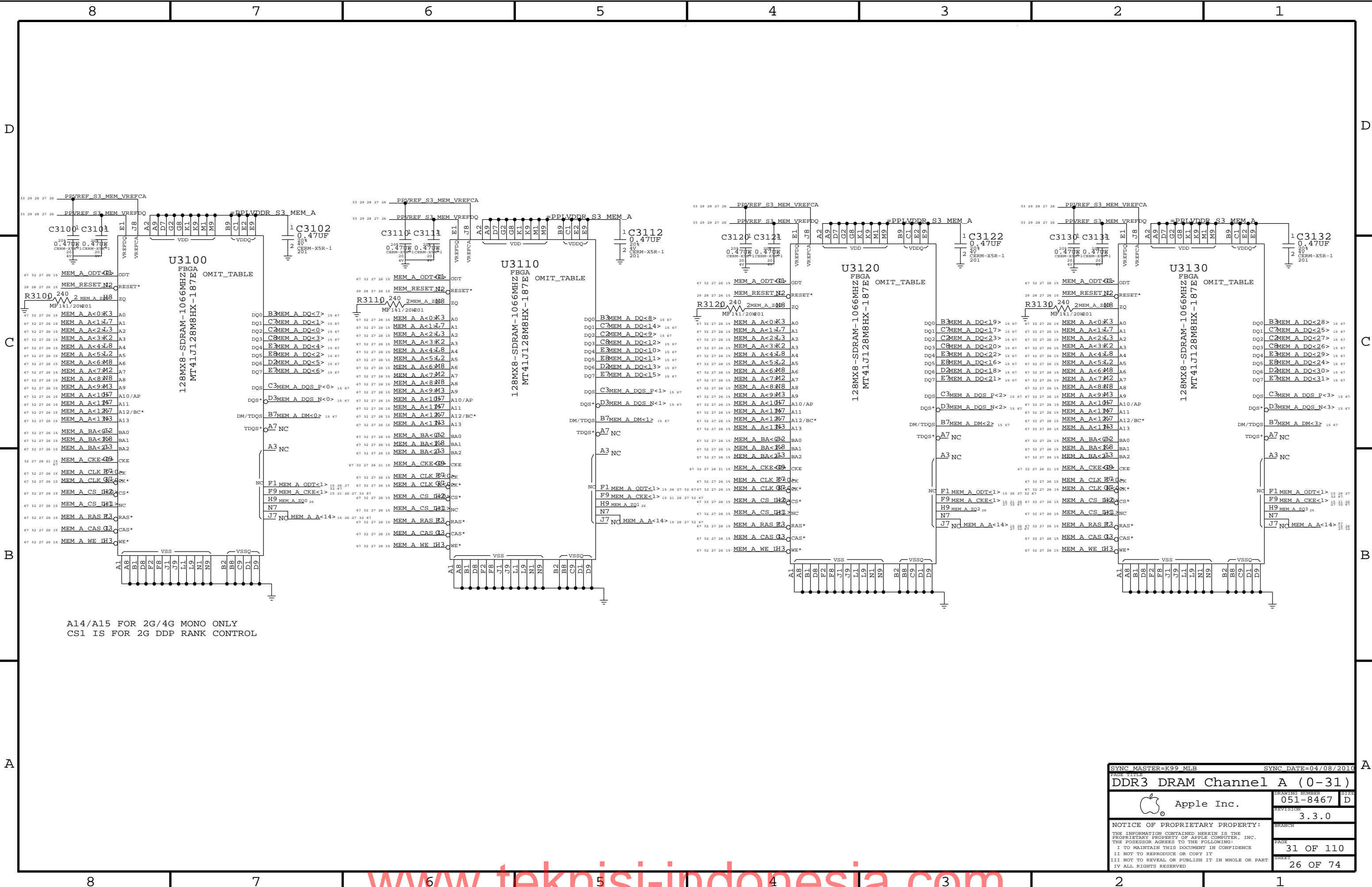
MCP S0 PWRGD & CPU_VLD




System Reset Circuit

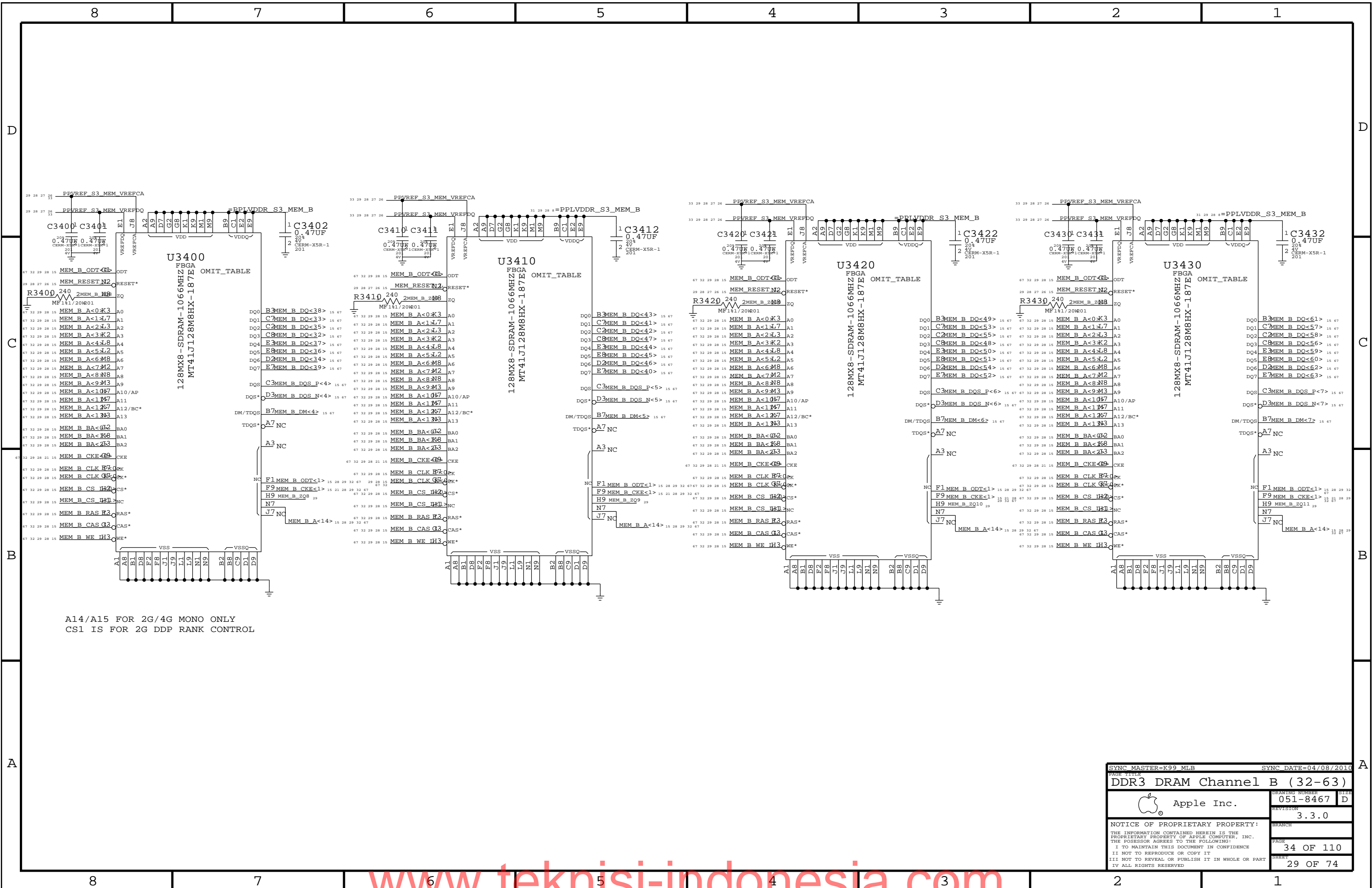


SYNC_MASTER=(K99_MLB)		SYNC_DATE=(02/11/2010)	
PAGE TITLE			
SB Misc			
		DRAWING NUMBER	
Apple Inc.		051-8467	
		SIZE	
		D	
		REVISION	
		3.3.0	
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
		BRANCH	
		PAGE	
		28 OF 110	
		SHEET	
		25 OF 74	




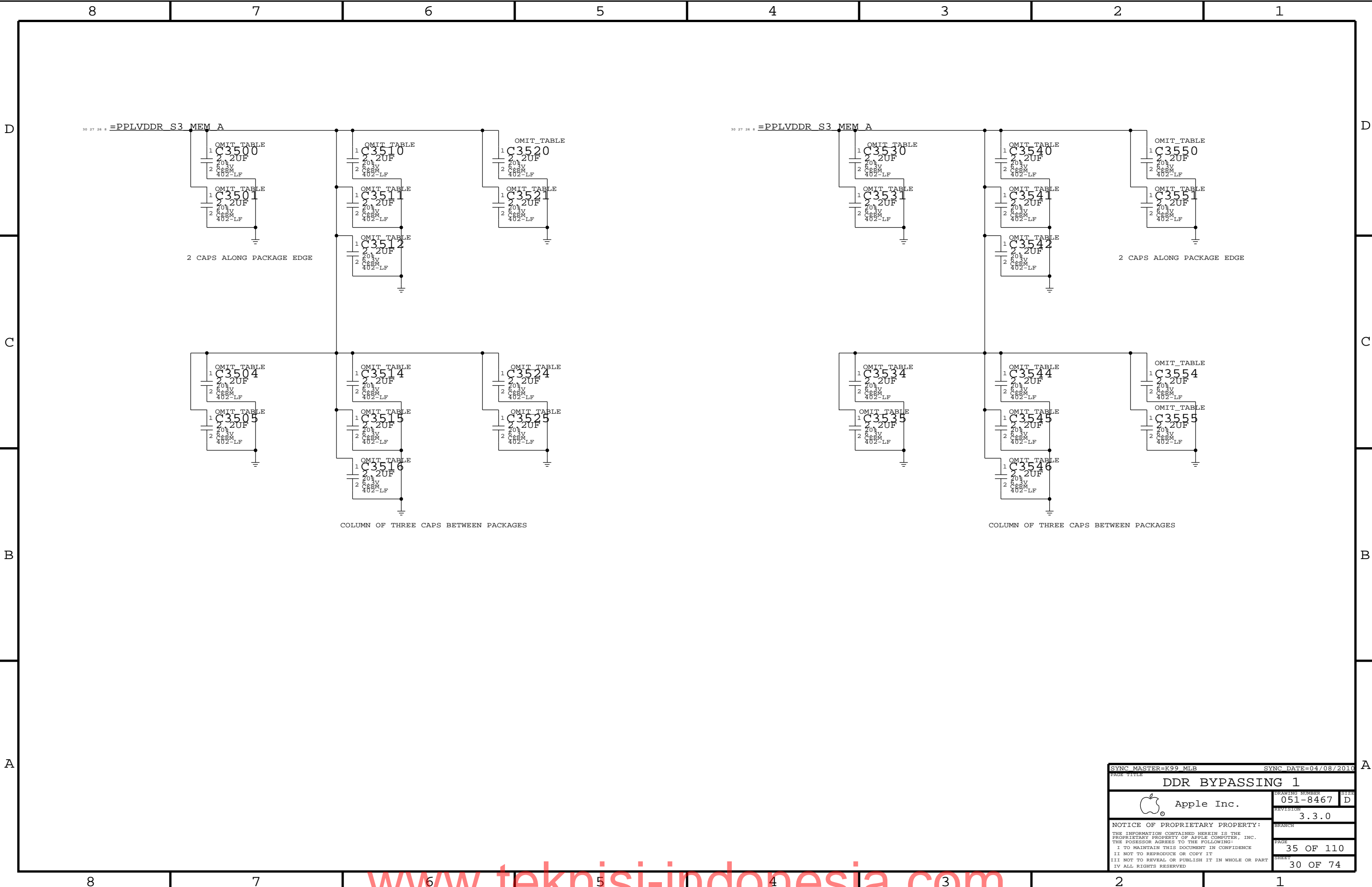
A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
DDR3 DRAM Channel A		(0-31)	
	Apple Inc.	DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	31 OF 110
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	26 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL


SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
DDR3 DRAM Channel B		B (32-63)	
	Apple Inc.	DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	34 OF 110
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	29 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



SYNC MASTER=K99 MLB

SYNC DATE=04/08/2010

DDR BYPASSING 1

 Apple Inc.

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

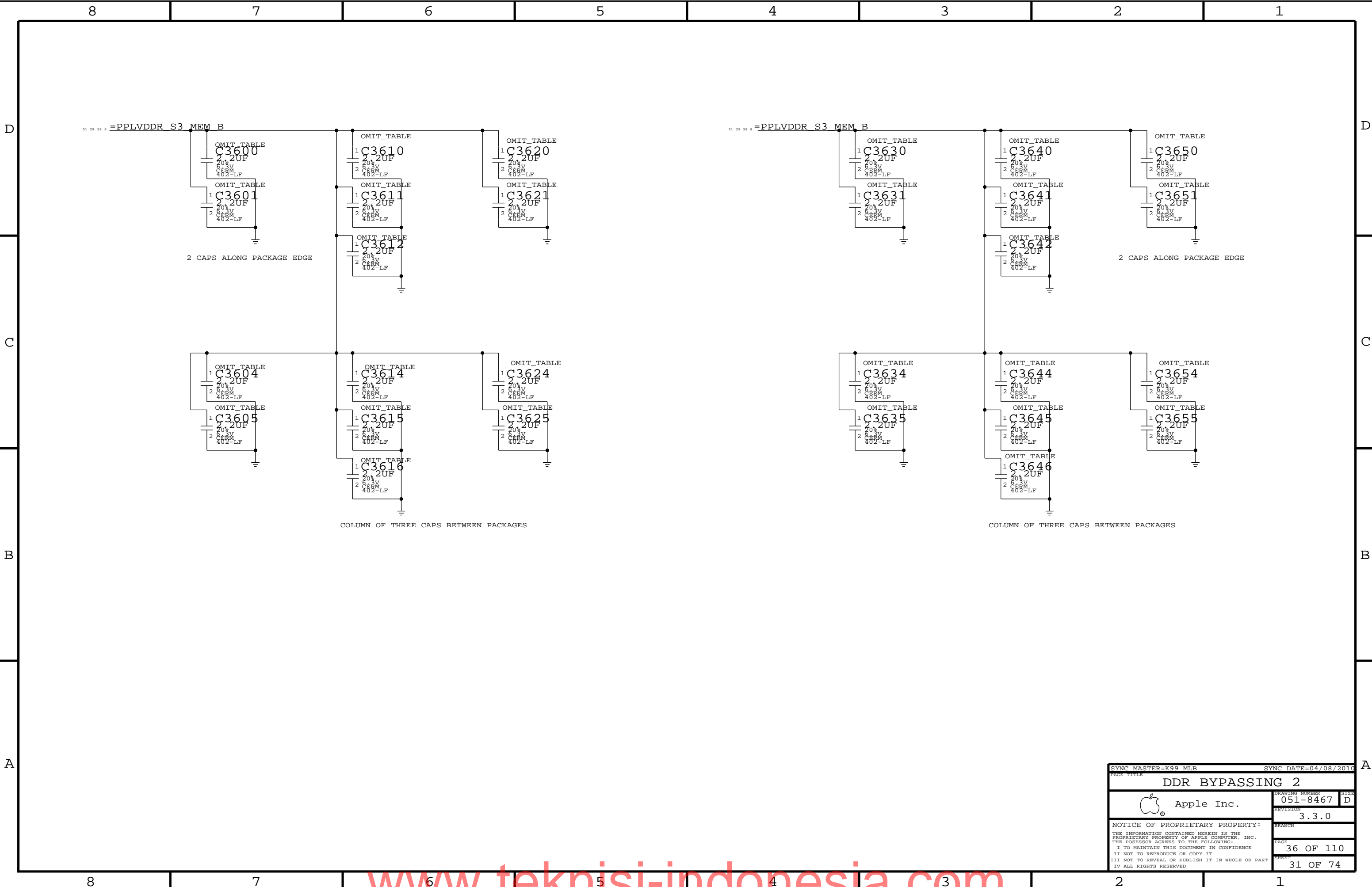
DRAWING NUMBER
051-8467

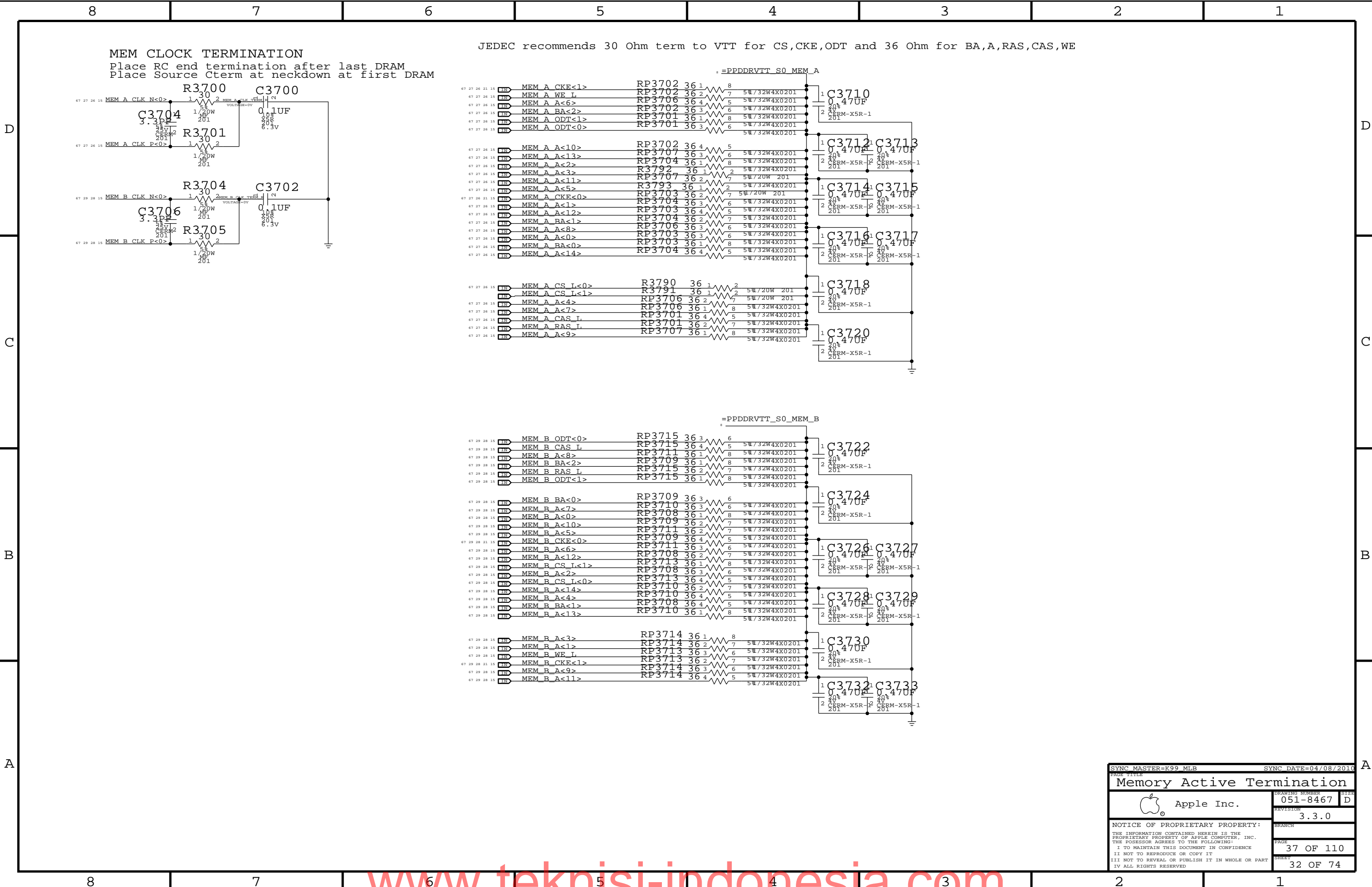
REVISION
3.3.0

BRANCH

PAGE
35 OF 110


SHEET
30 OF 74





JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

MEM CLOCK TERMINATION
Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
Memory Active Termination			
 Apple Inc.	DRAWING NUMBER	051-8467	SIZE
	REVISION	3.3.0	D
	BRANCH		
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
PAGE		37 OF 110	
SHEET		32 OF 74	

D

C

B

A

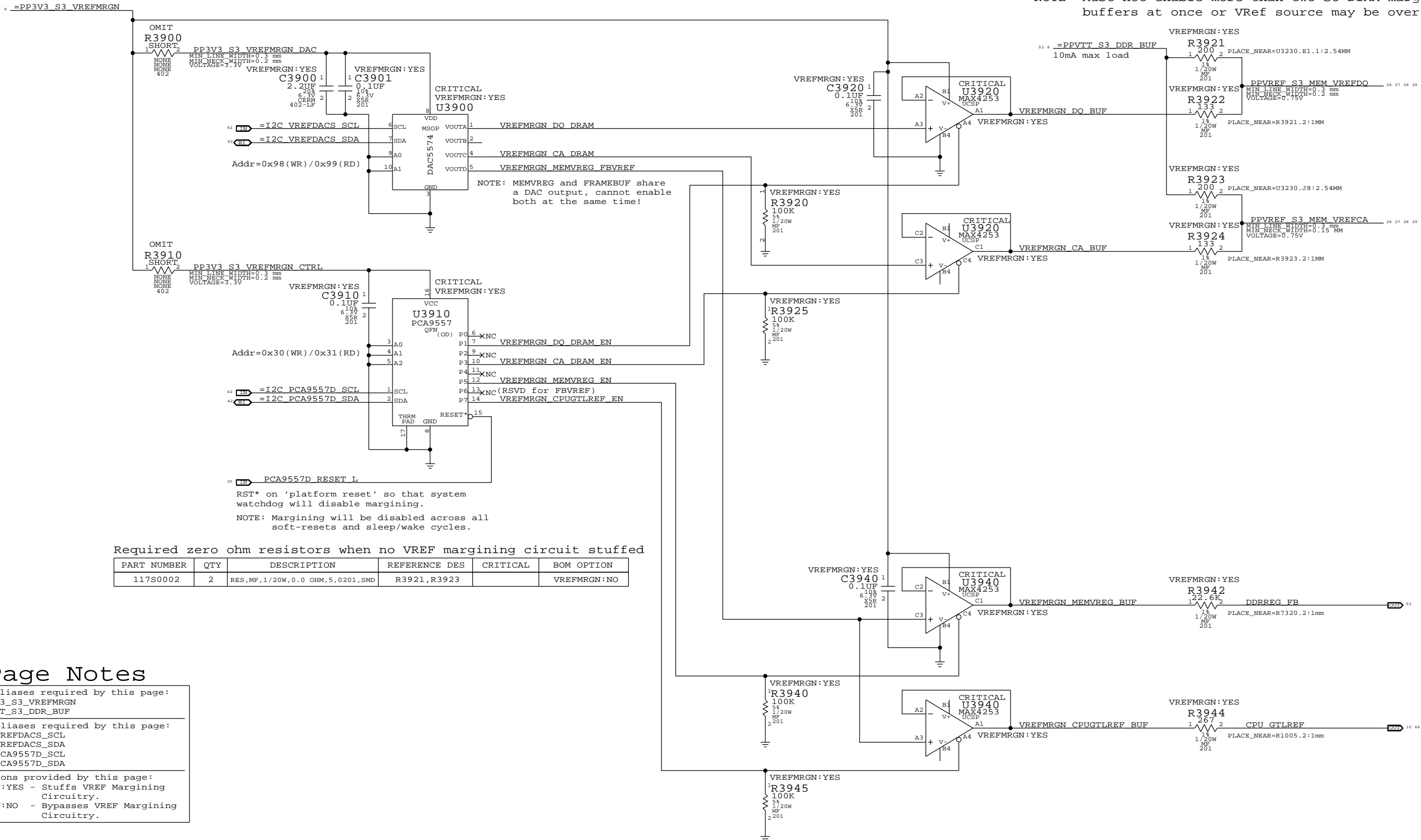
D

C

B

A

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	2	RES, MF, 1/20W, 0.0 OHM, 5, 0201, SMD	R3921, R3923		VREFMRGN:NO


Page Notes

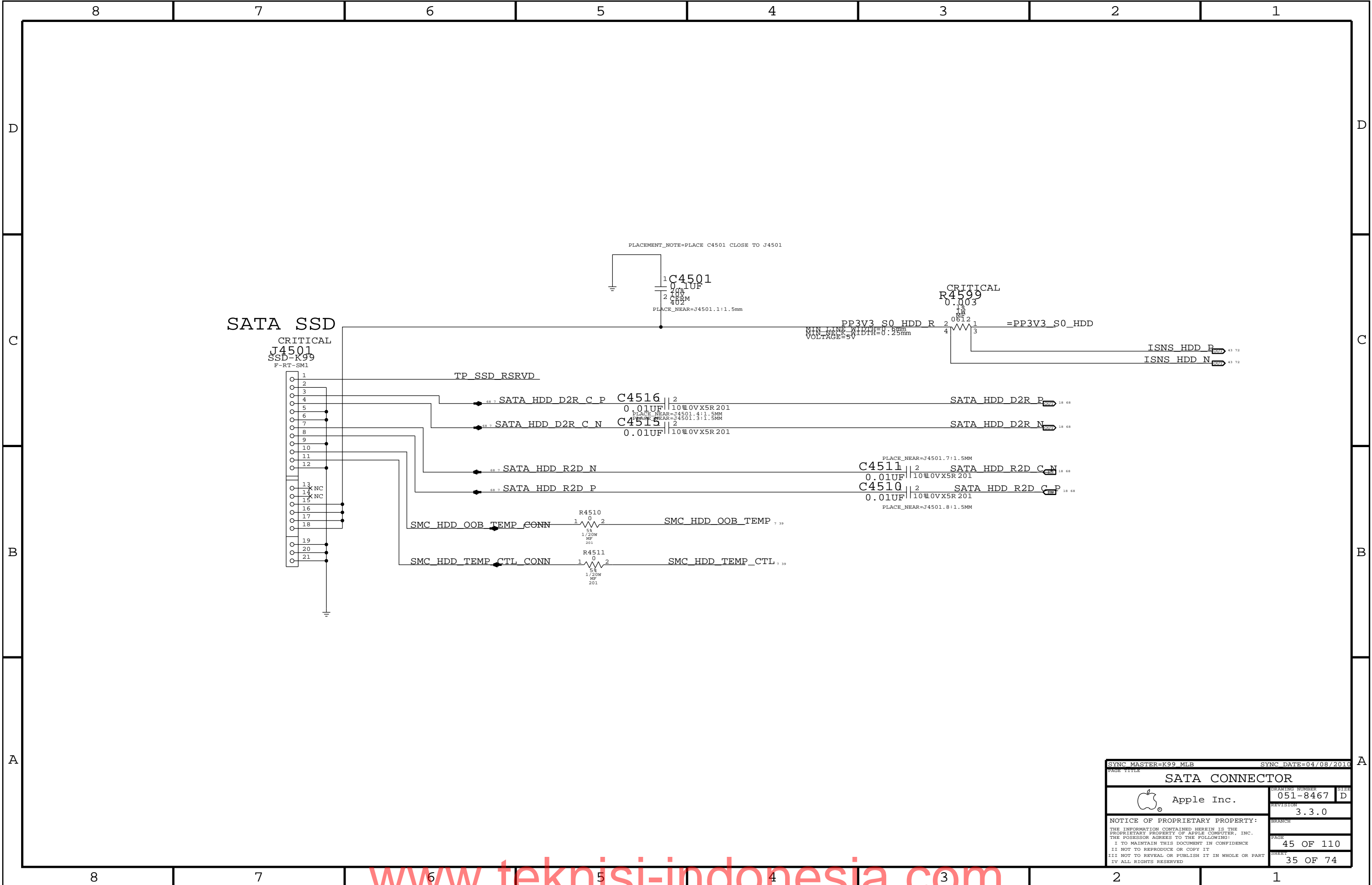
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF


Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN:YES - Stuffs VREF Margining Circuitry.
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM VREF DQ	MEM VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	C	D	D
PCA9557D Pin:	1	3	5	7
Nominal value		0.75V (DAC: 0x3A)	1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)	1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
Vref current:		+3.4mA - -3.4mA (- = sourced)	+33uA - -528uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output	8.59mV / step @ output	9.24mV / step @ output

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
FSB/DDR3 Vref		Margining	
		DRAWING NUMBER	051-8467
Apple Inc.		D	
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	39 OF 110
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	33 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
SATA CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	45 OF 110
		SHEET	35 OF 74
		SIZE	D

D

C

B

A

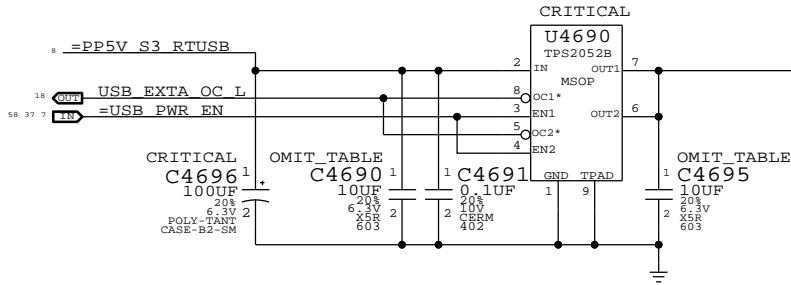
D

C

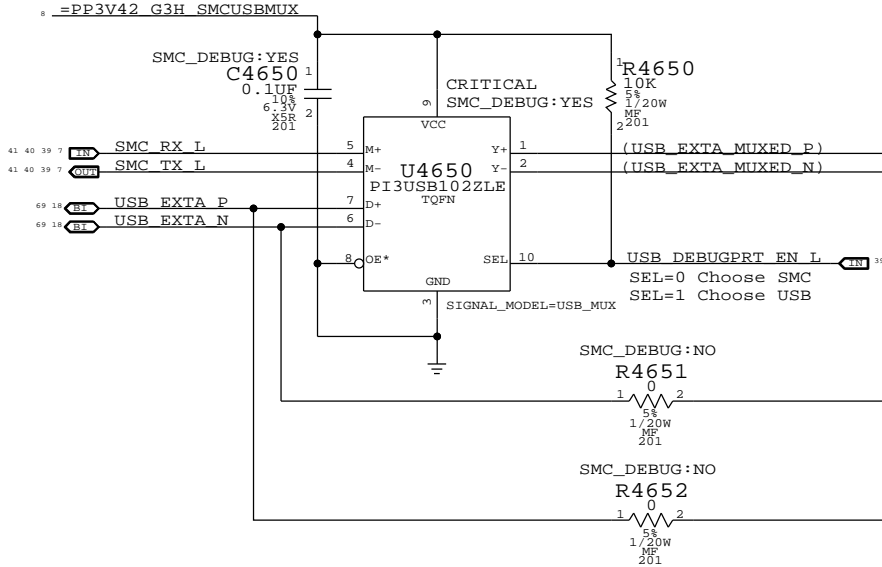
B

A

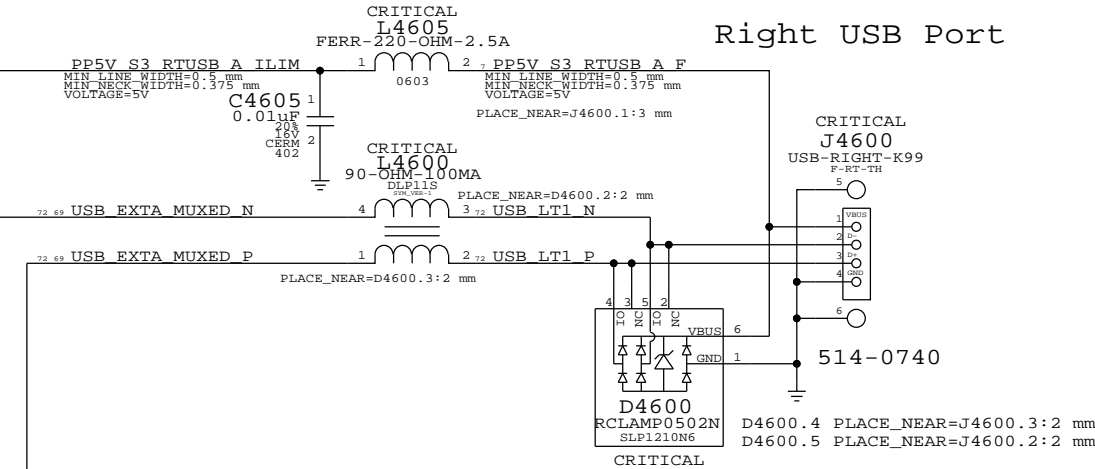
Port Power Switch




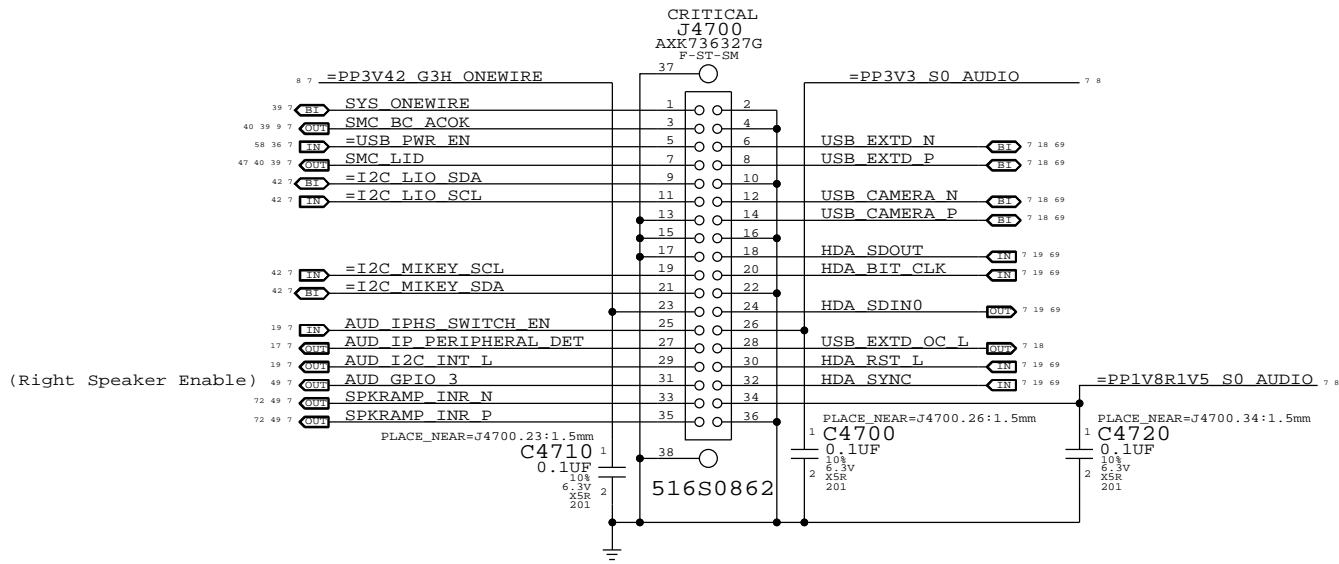
USB/SMC Debug Mux




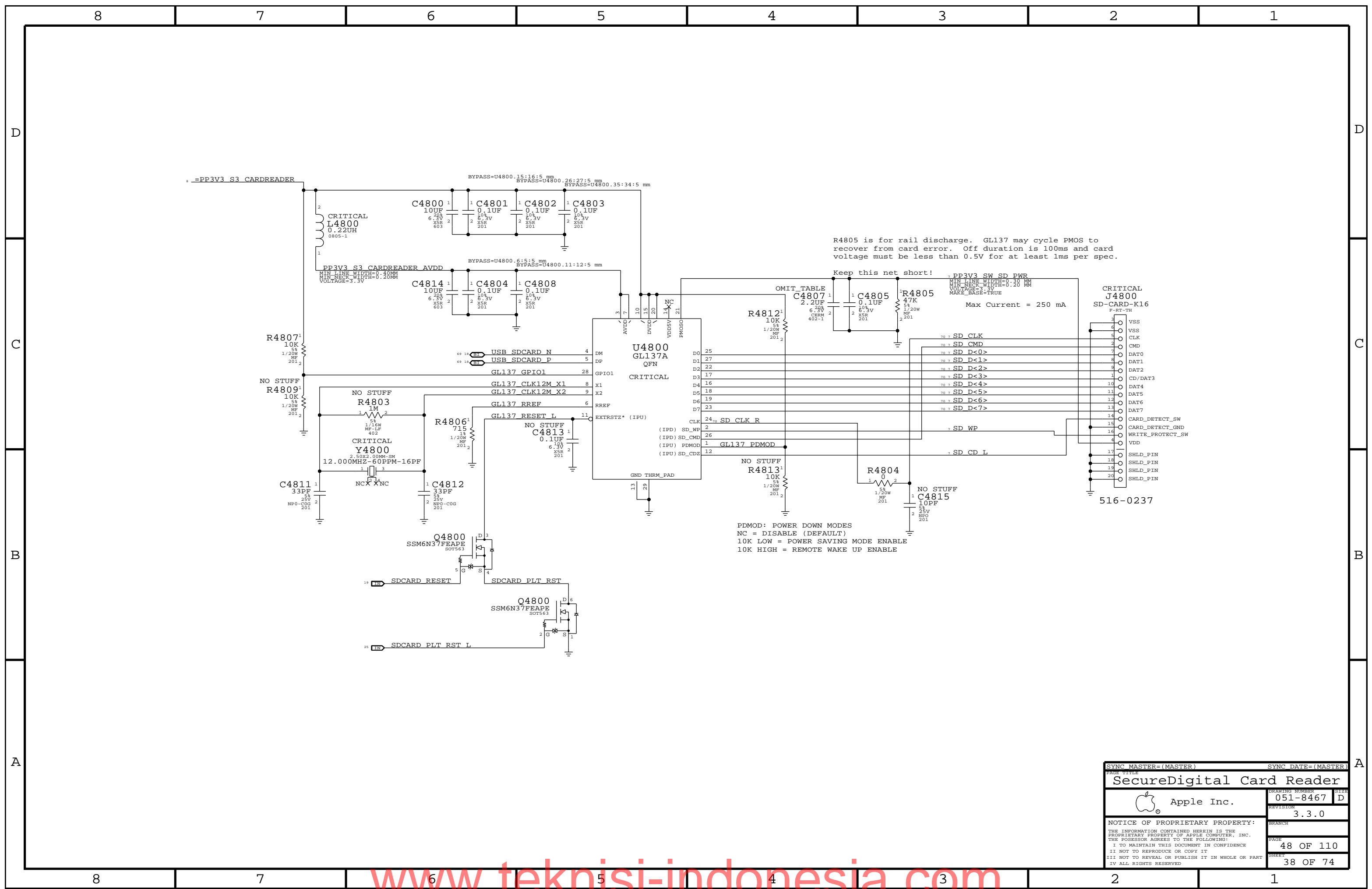
Right USB Port



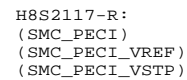
SYNC MASTER=K99 MLB		SYNC DATE=03/01/2010	
PAGE TITLE			
External USB Connectors			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	46 OF 110
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	36 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			




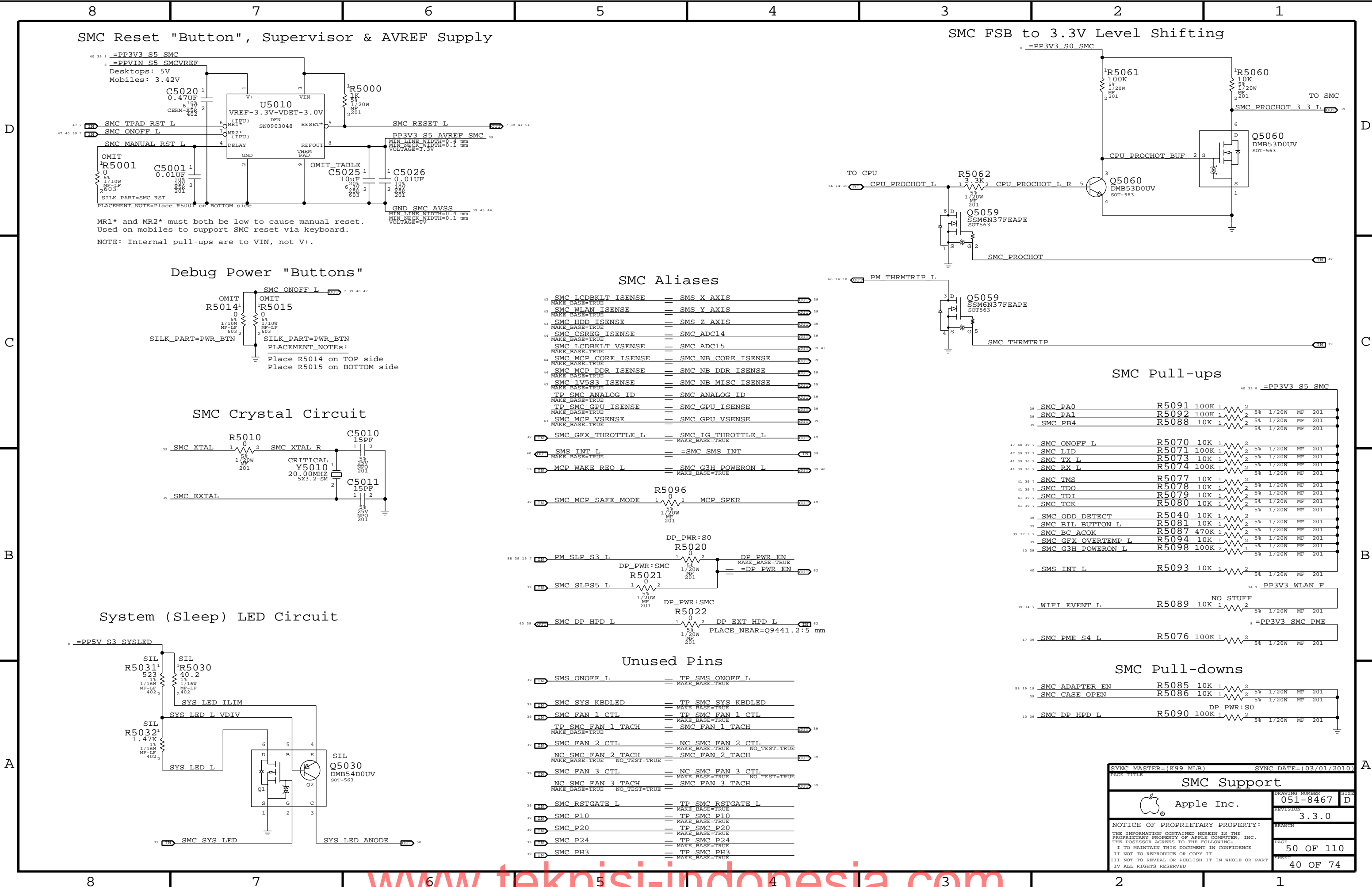
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)	
PAGE TITLE			
Left I/O (LIO) Connector		Drawing Number	
 Apple Inc.		051-8467	D
		REVISION	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		3.3.0	
		BRANCH	
		PAGE	
		SHEET	
		47 OF 110	37 OF 74

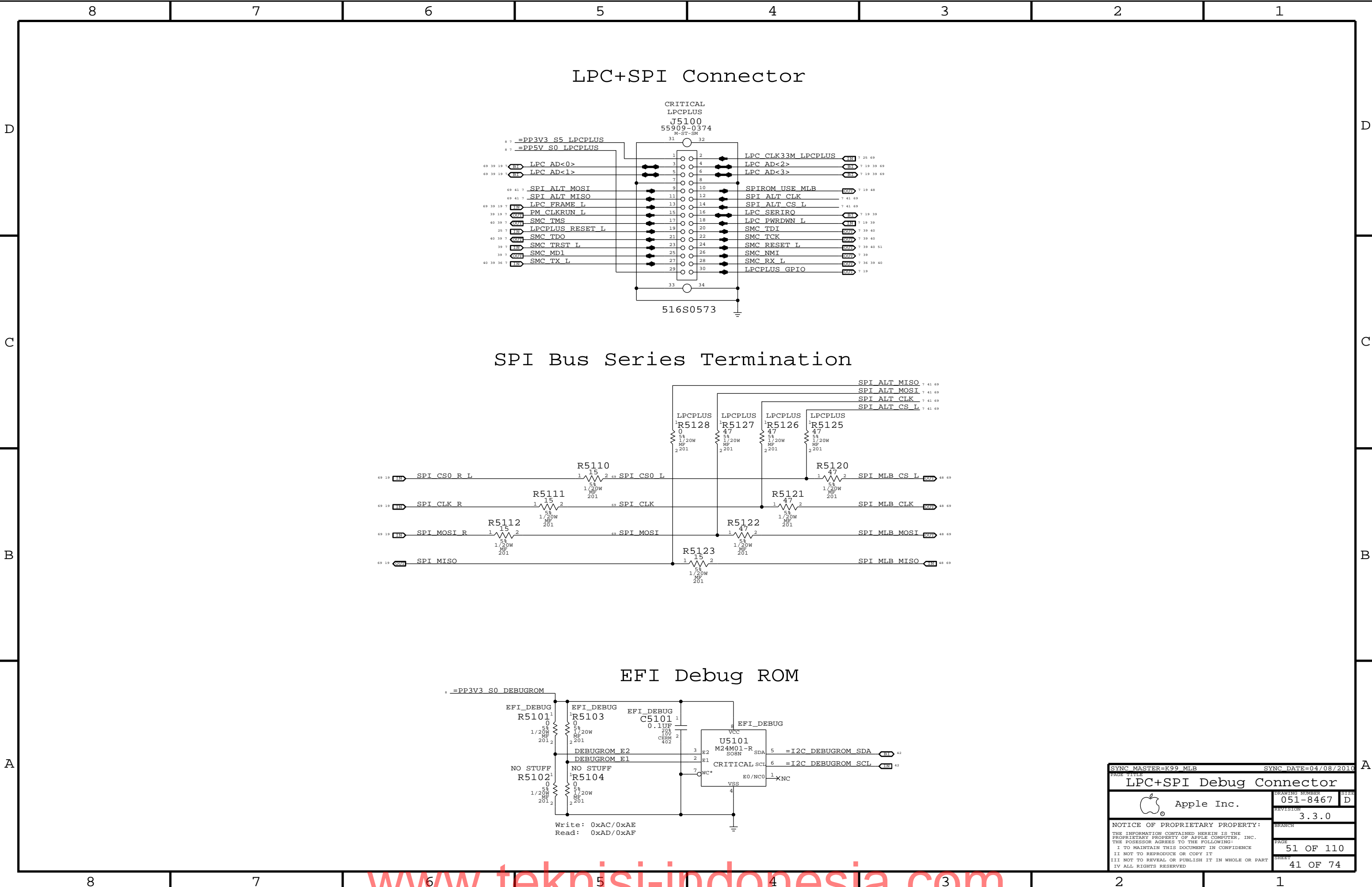


A

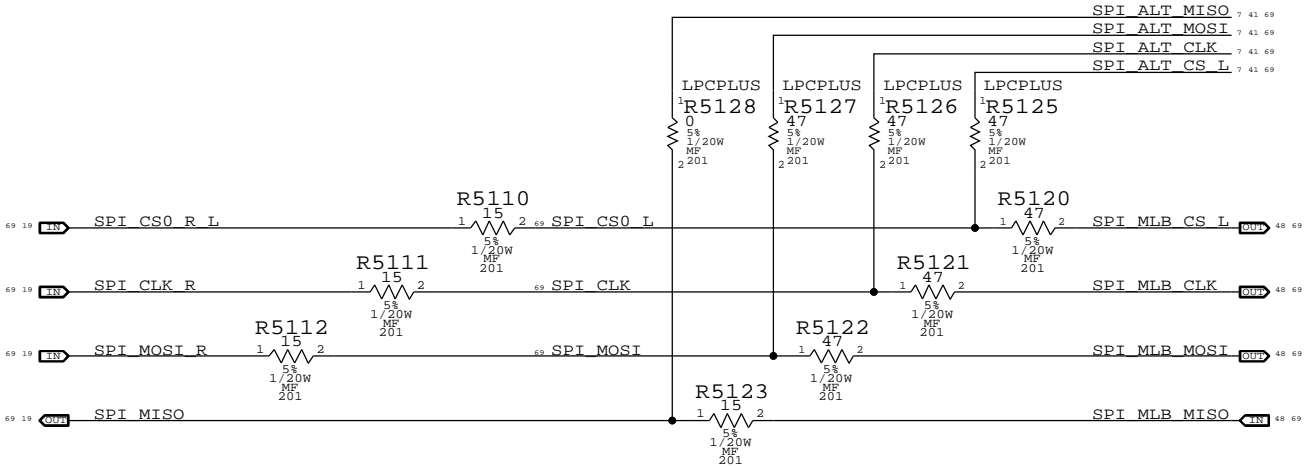


SYNC MASTER-K16 MLB		SYNC DATE=06/01/2010	
PAGE TITLE			
SMC			
 Apple Inc.		DRAWING NUMBER 051-8467	
		SIZE D	
		REVISION 3.3.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		49 OF 110	
		SHEET 39 OF 74	

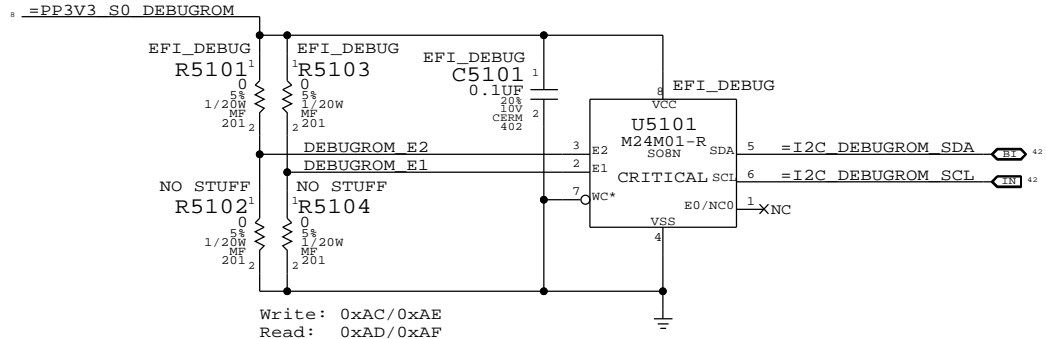





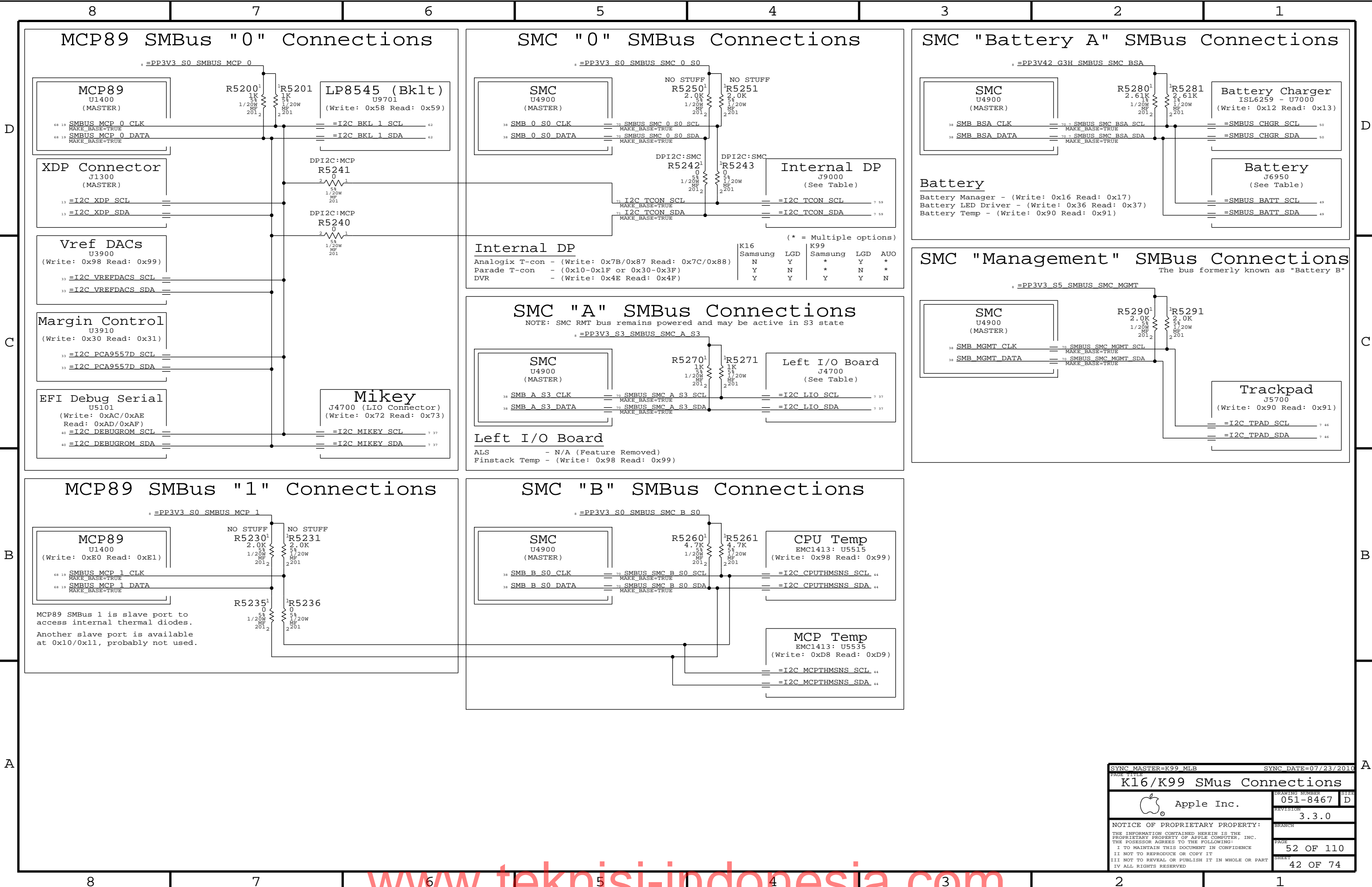
SPI Bus Series Termination

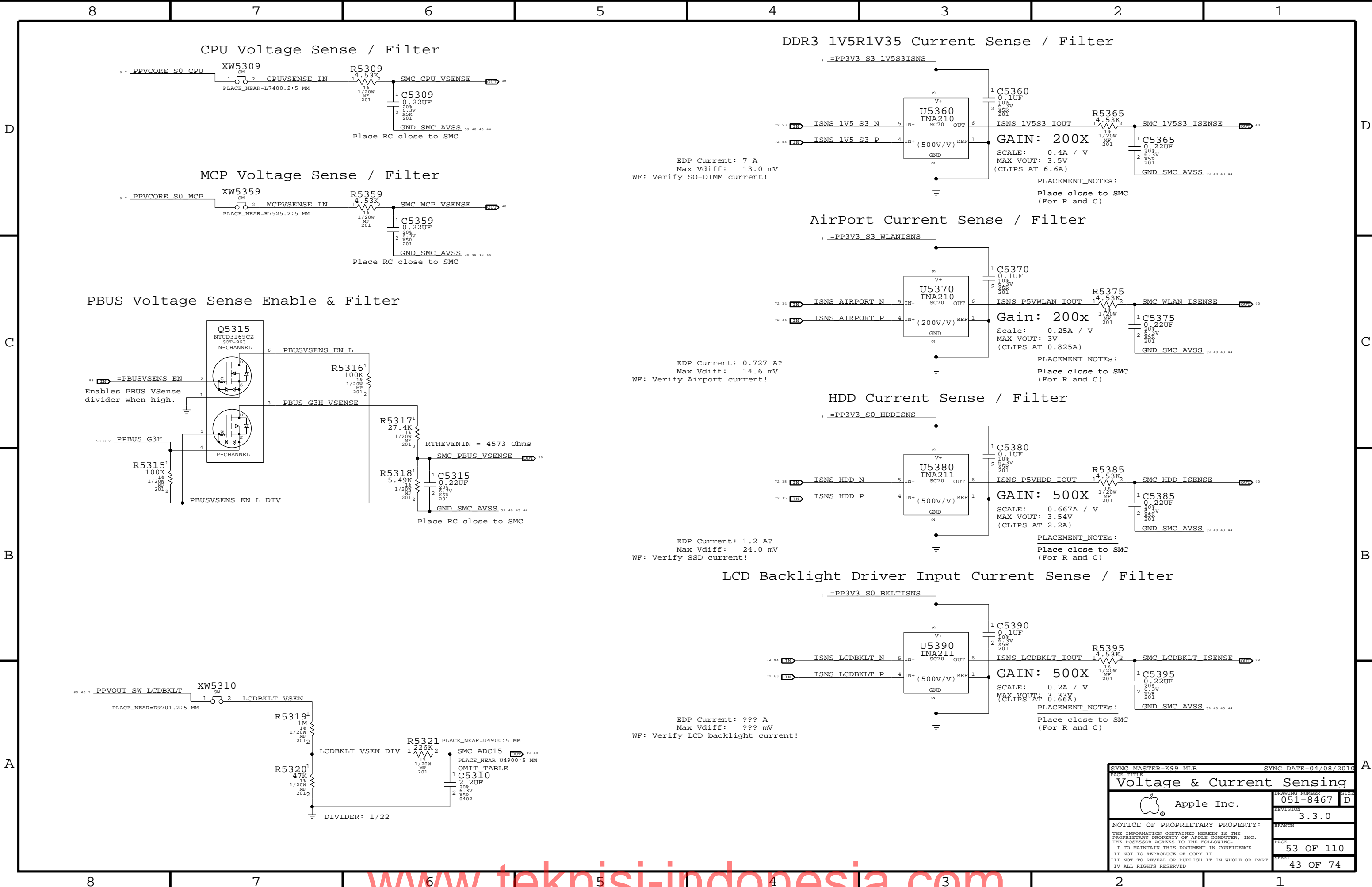


EFI Debug ROM

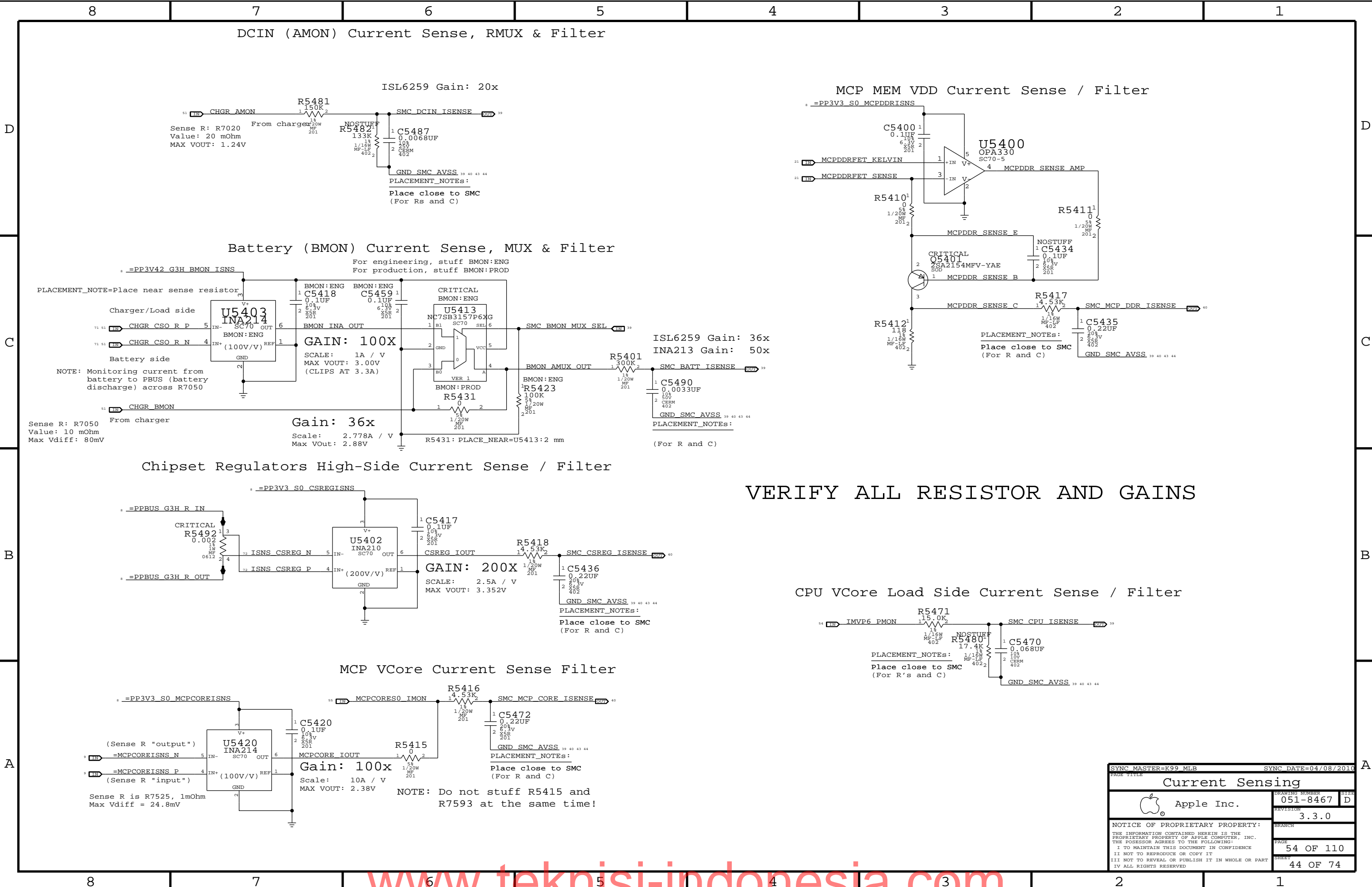


SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
LPC+SPI Debug Connector			
 Apple Inc.		DRAWING NUMBER	051-8467
		SIZE	D
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	51 OF 110
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	41 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			






SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE		Voltage & Current Sensing	
DRAWING NUMBER		051-8467	SIZE D
REVISION		3.3.0	BRANCH
NOTICE OF PROPRIETARY PROPERTY:		PAGE	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		53 OF 110	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	
II NOT TO REPRODUCE OR COPY IT		43 OF 74	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



VERIFY ALL RESISTOR AND GAINS

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
Current Sensing			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	54 OF 110
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	44 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			

D

C

B

A

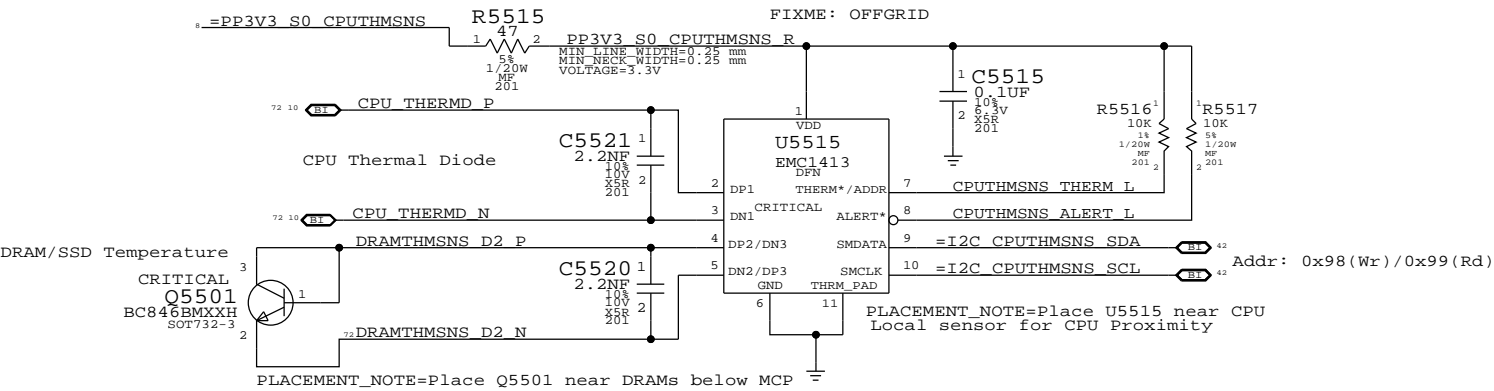
D

C

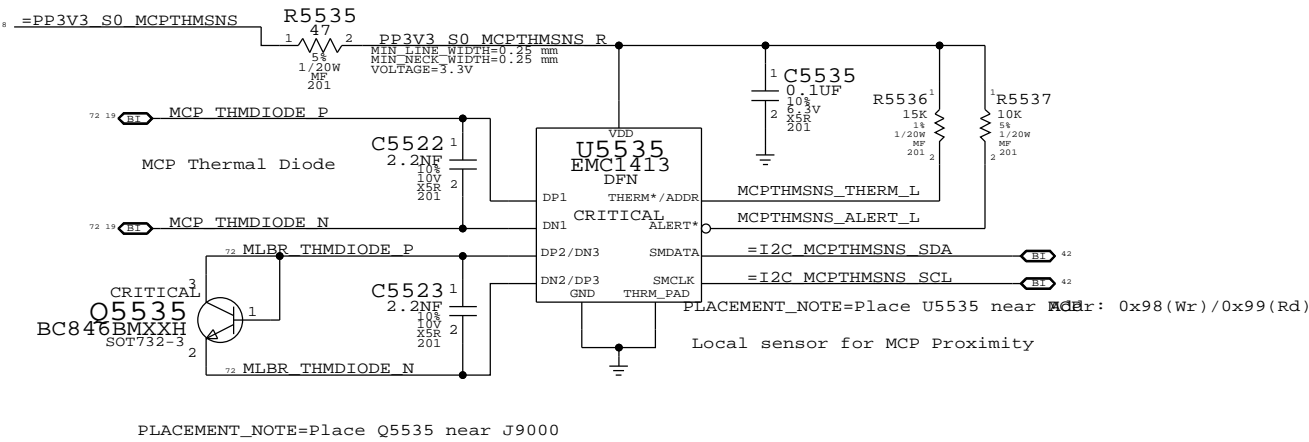
B


A

CPU T-Diode Thermal Sensor

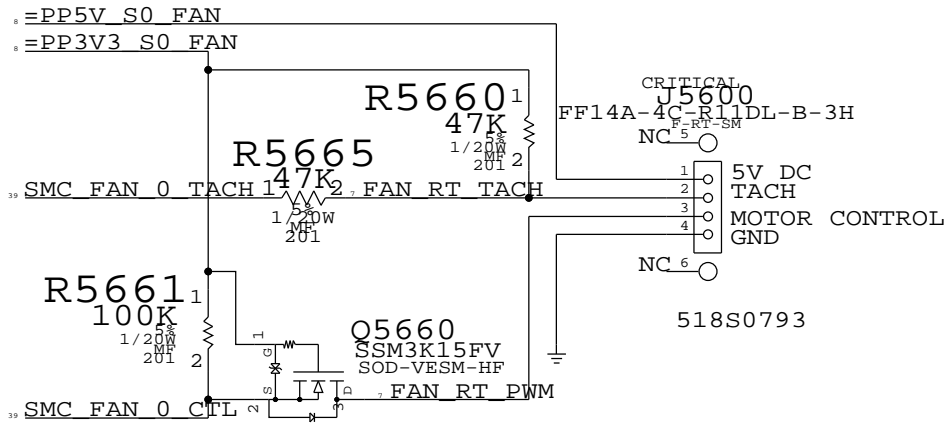


MCP T-Diode Thermal Sensor

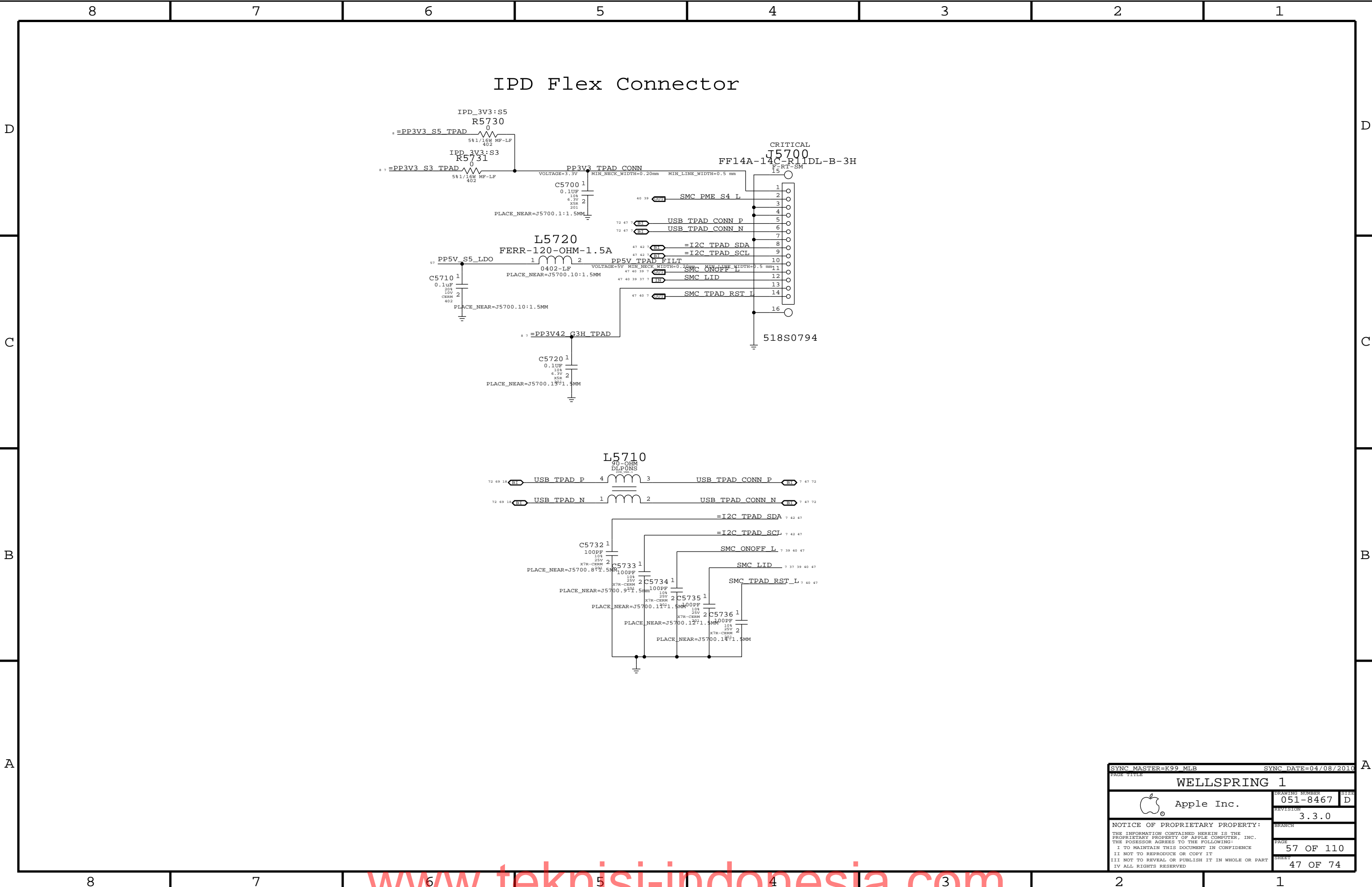



SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
Thermal Sensors			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	55 OF 110
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	45 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			

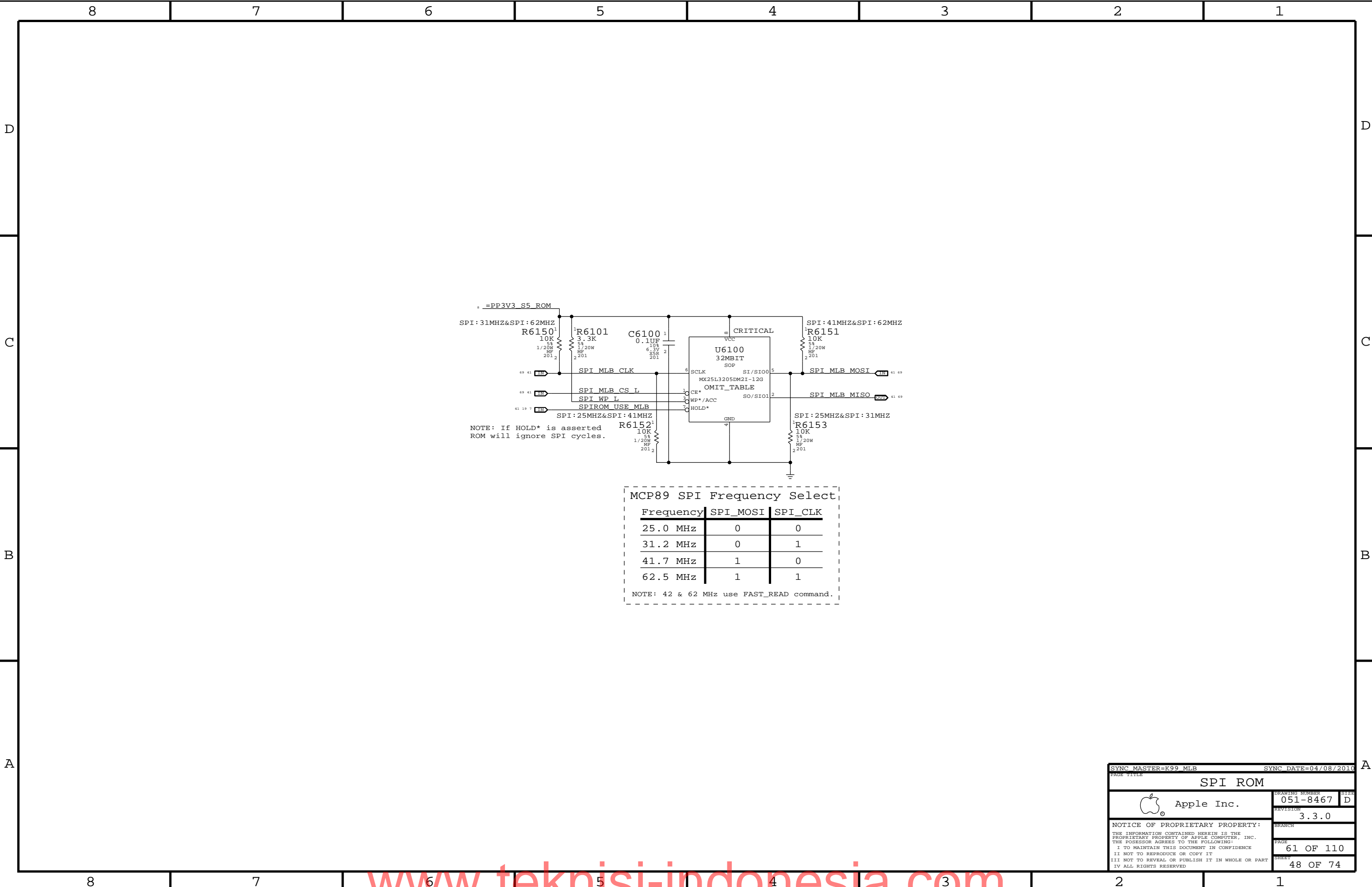
FAN CONNECTOR



SYNC_MASTER=K99_MLB		SYNC_DATE=04/08/2010	
PAGE_TITLE		Fan	
		DRAWING_NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	56 OF 110
		SHEET	46 OF 74



SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
WELLSPRING 1			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	57 OF 110
		SHEET	47 OF 74



MCP89 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1
NOTE: 42 & 62 MHz use FAST_READ command.		

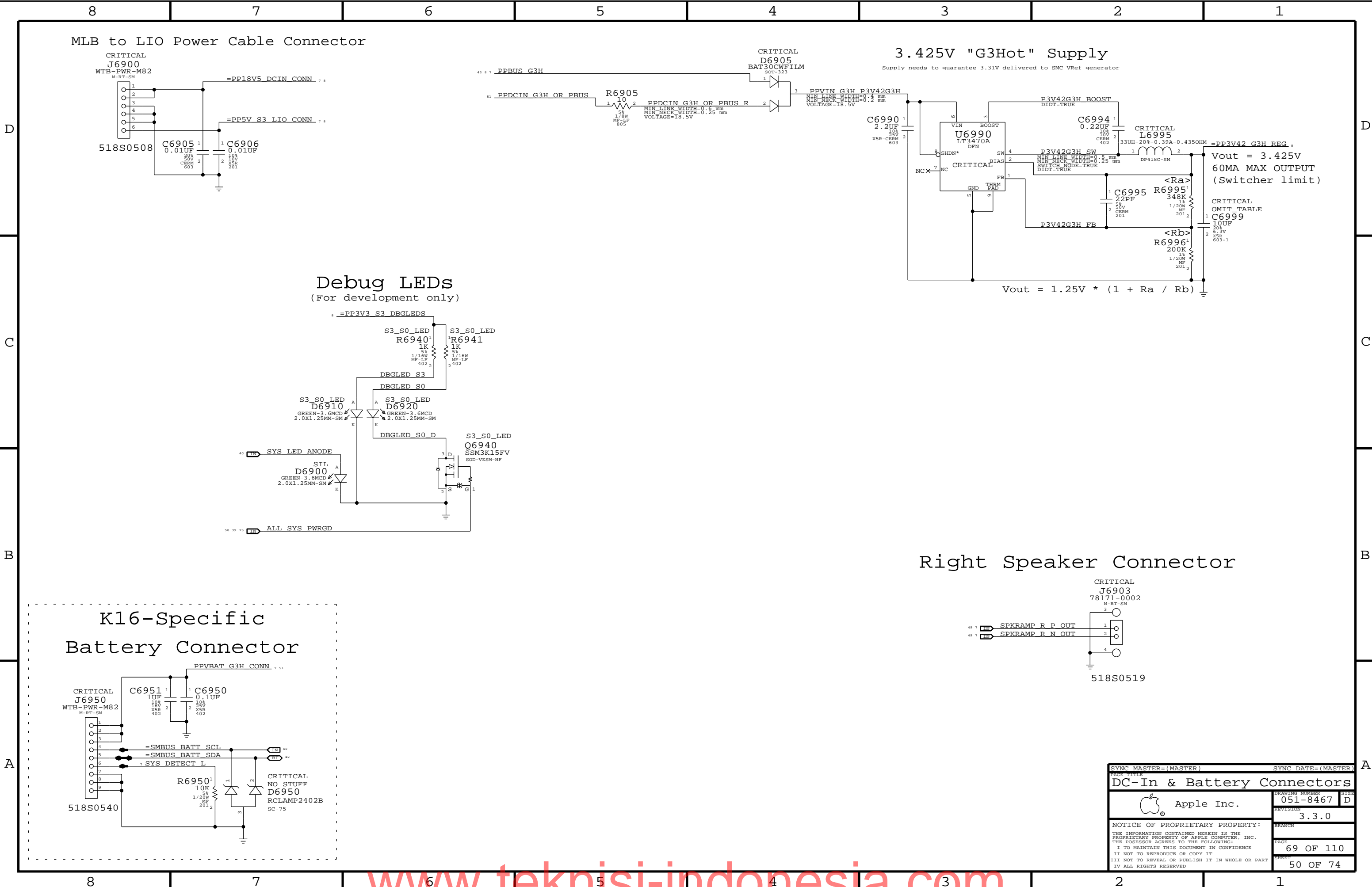
www.teknisi-indonesia.com

www.teknisi-indonesia.com

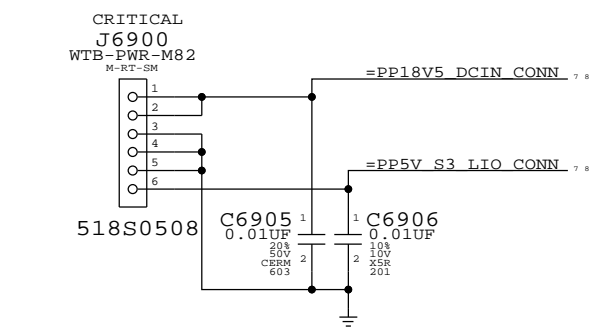
www.teknisi-indonesia.com

www.teknisi-indonesia.com



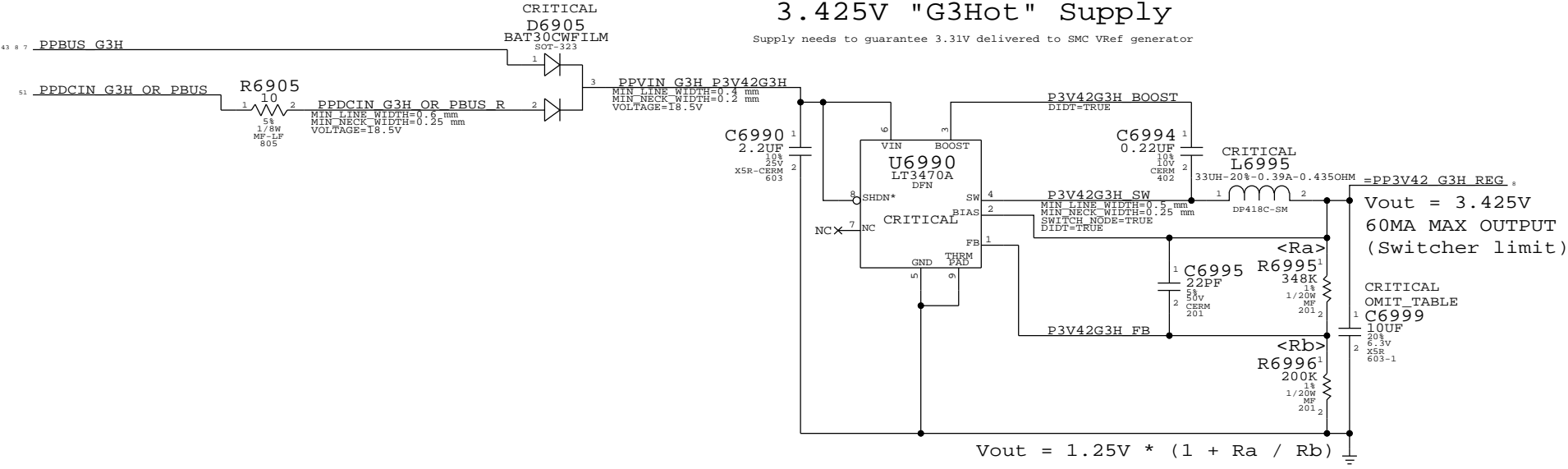


MLB to LIO Power Cable Connector



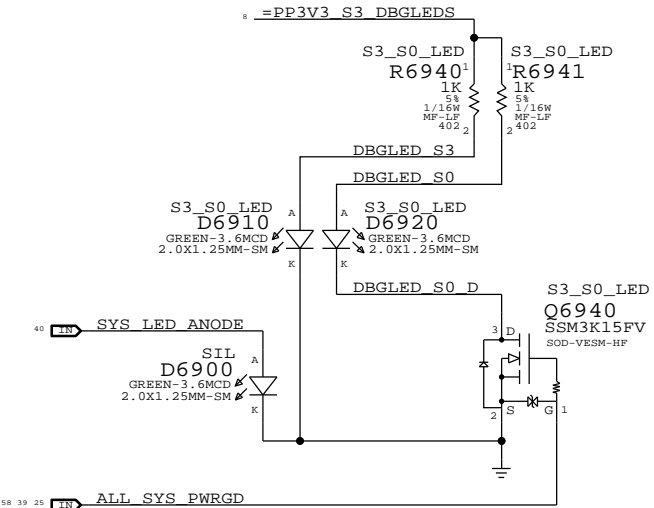
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

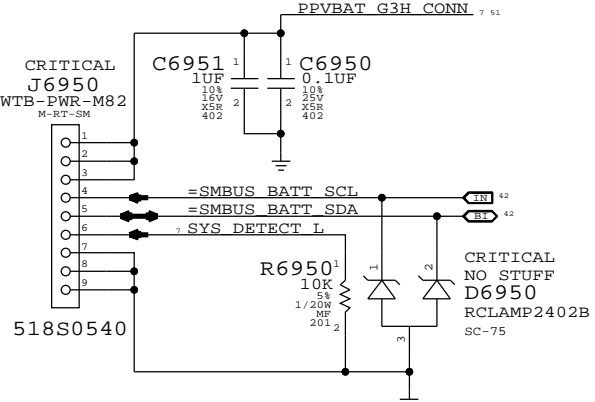


Debug LEDs

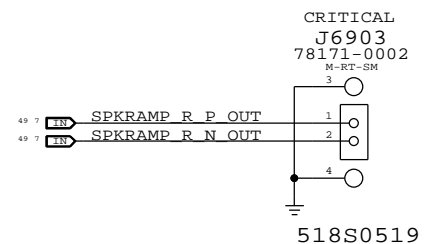
(For development only)



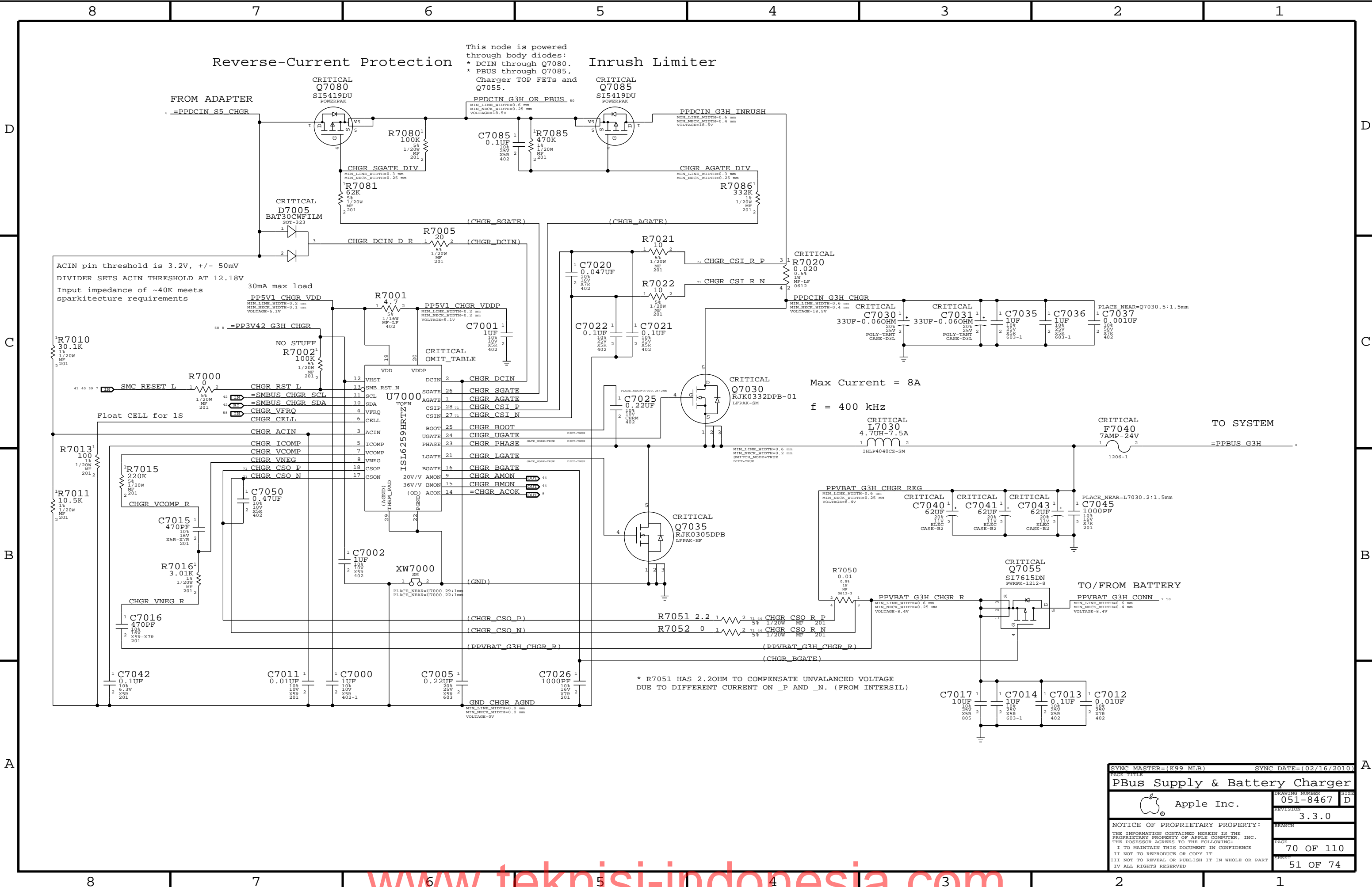
K16-Specific Battery Connector




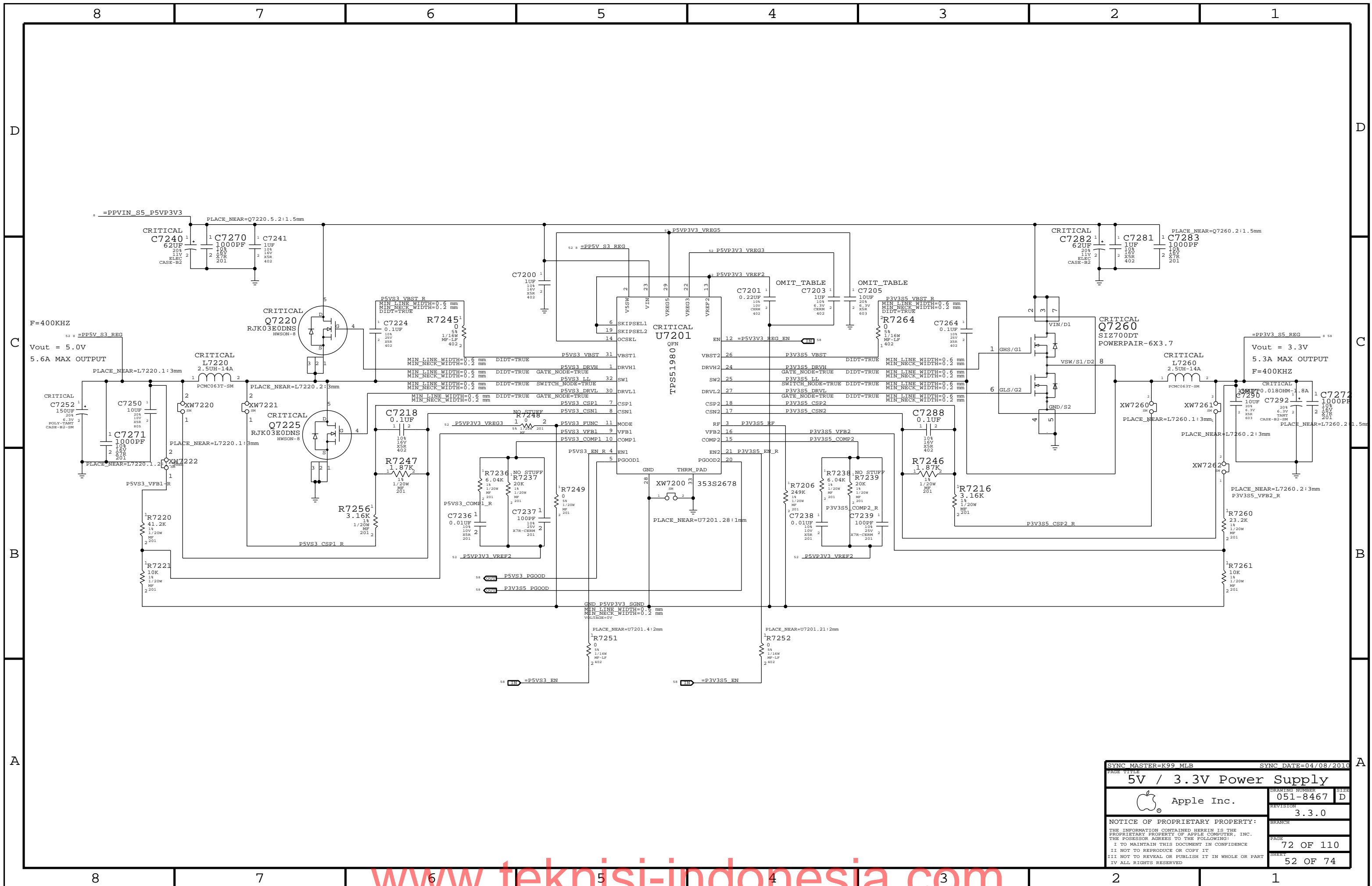
Right Speaker Connector




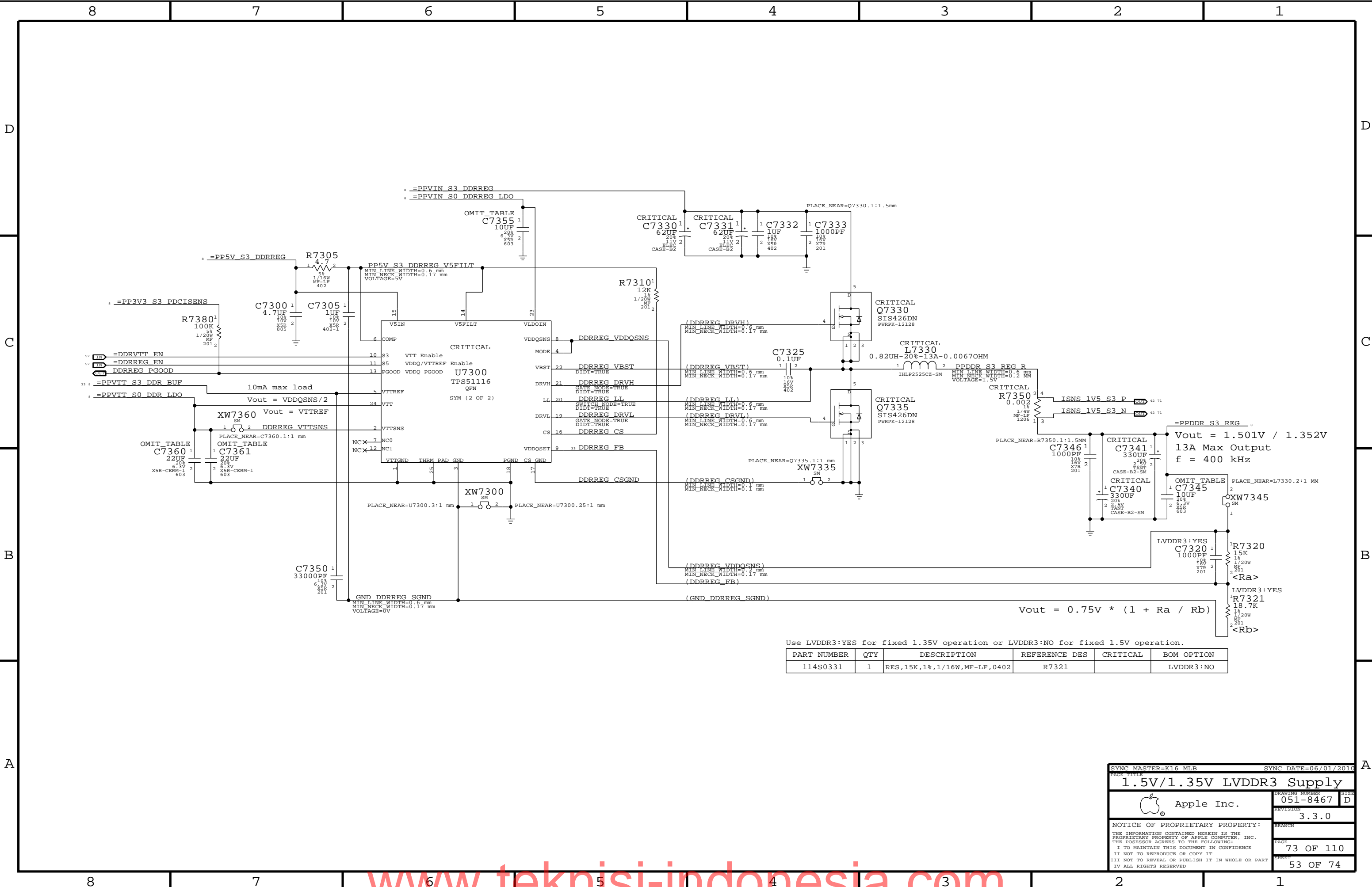
SYNC MASTER=(MASTER)		SYNC DATE=(MASTER)	
PAGE TITLE		DRAWING NUMBER	
DC-In & Battery Connectors		051-8467	
Apple Inc.		REVISION	3.3.0
		BRANCH	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		PAGE	69 OF 110
		SHEET	50 OF 74



SYNC MASTER=(K99 MLB)		SYNC DATE=(02/16/2010)	
PAGE TITLE			
PBus Supply & Battery Charger			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	70 OF 110
		SHEET	51 OF 74




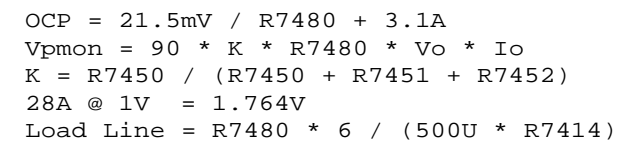
SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
5V / 3.3V Power Supply			
 Apple Inc.		DRAWING NUMBER	051-8467
		SIZE	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	3.3.0
		BRANCH	
PAGE		72	OF 110
SHEET		52	OF 74




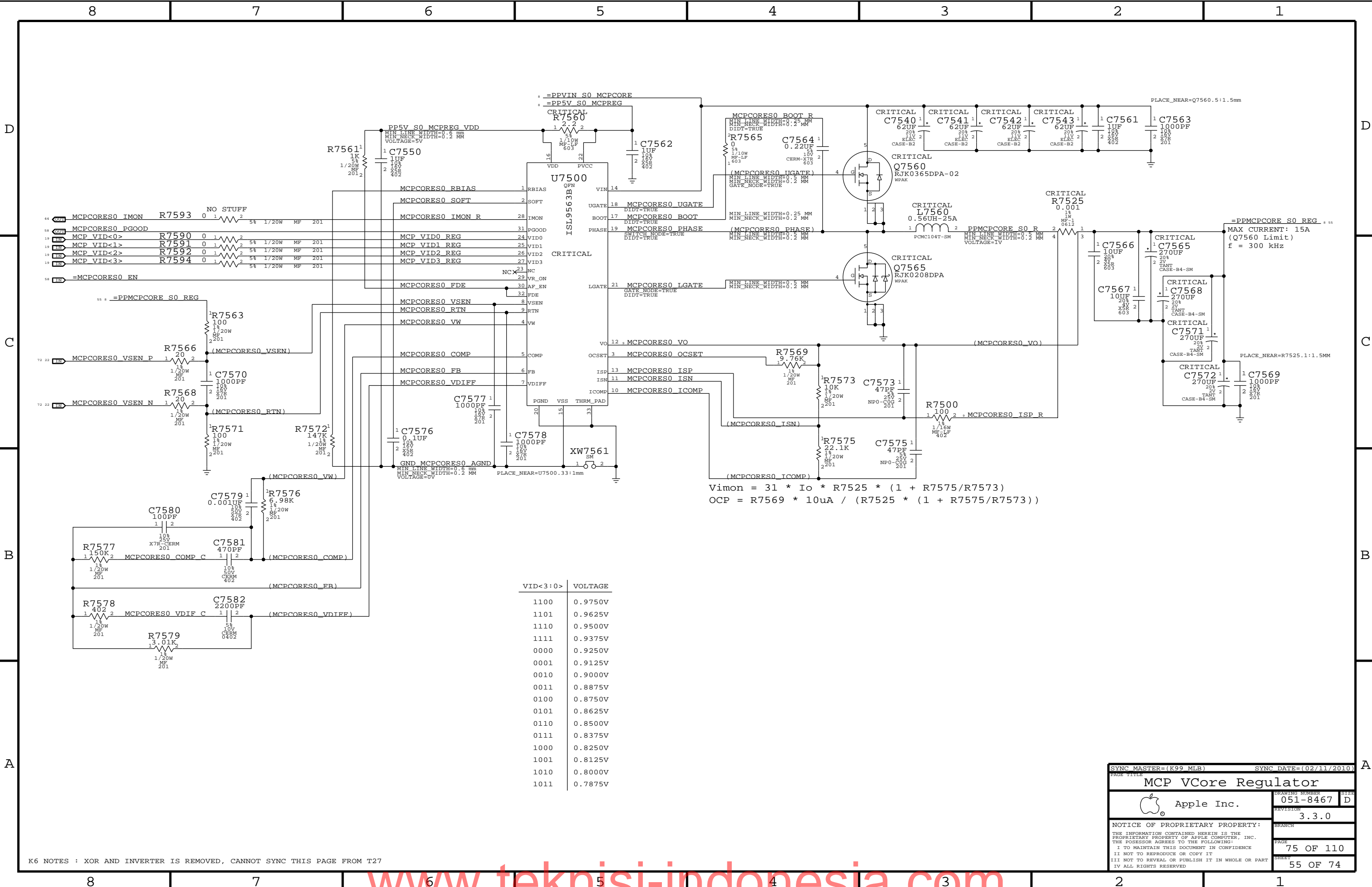
Use LVDDR3:YES for fixed 1.35V operation or LVDDR3:NO for fixed 1.5V operation.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0331	1	RES,15K,1%,1/16W,MF-LF,0402	R7321		LVDDR3:NO

SYNC MASTER=K16 MLB		SYNC DATE=06/01/2010	
PAGE TITLE			
1.5V/1.35V LVDDR3 Supply		DRAWING NUMBER	
 Apple Inc.		051-8467	
		REVISION	
		3.3.0	
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
		BRANCH	
		PAGE	
		73 OF 110	
		SHEET	
		53 OF 74	

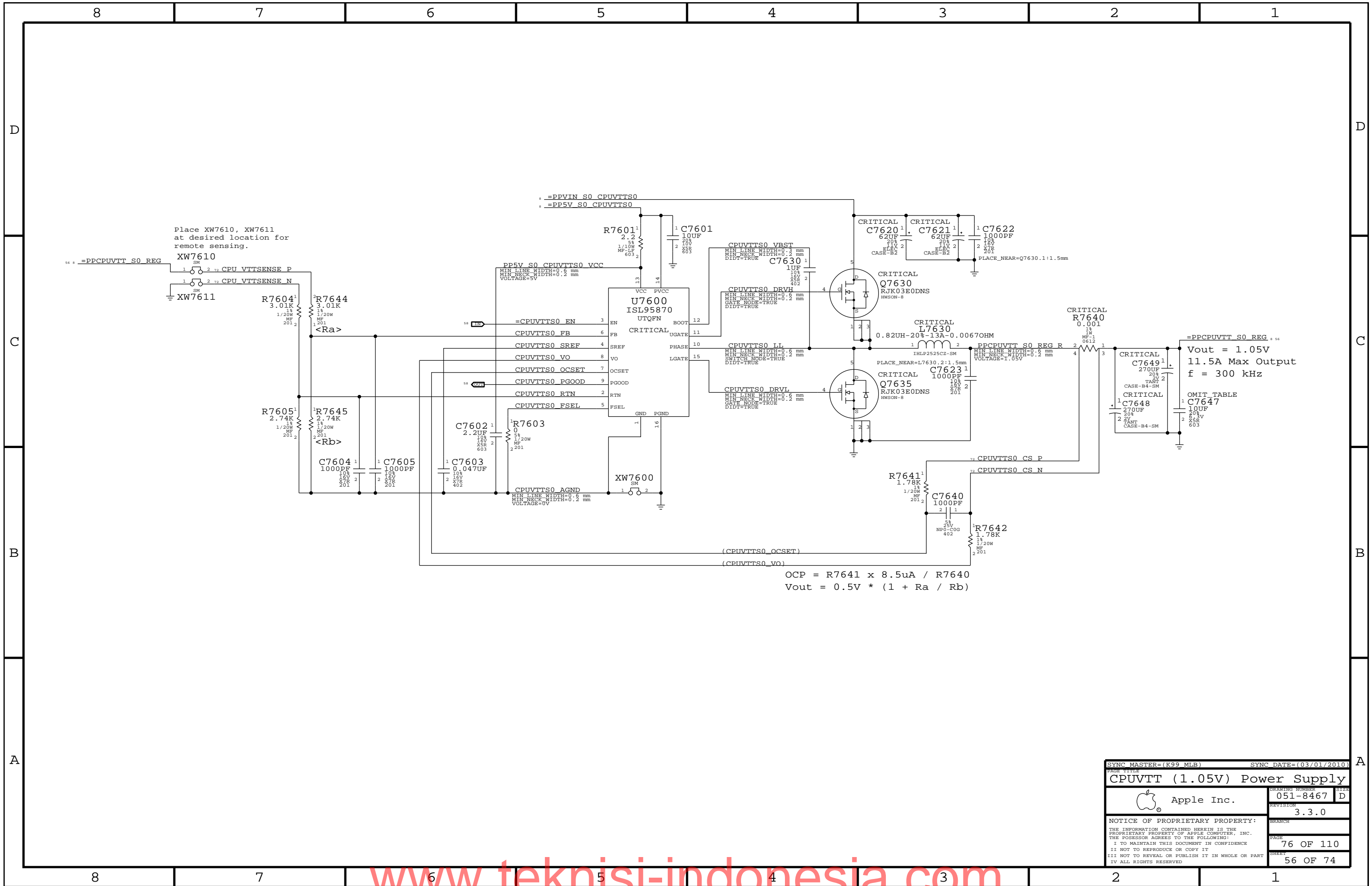


SYNC MASTER=(K99 MLB)		SYNC DATE=(02/16/2010)	
P/N: IMVP6 CPU VCore Regulator			
 Apple Inc.		DRAWING NUMBER 051-8467	SIZE D
		REVISION 3.3.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I WILL NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED		PAGE 74 OF 110	
		SHEET 54 OF 74	

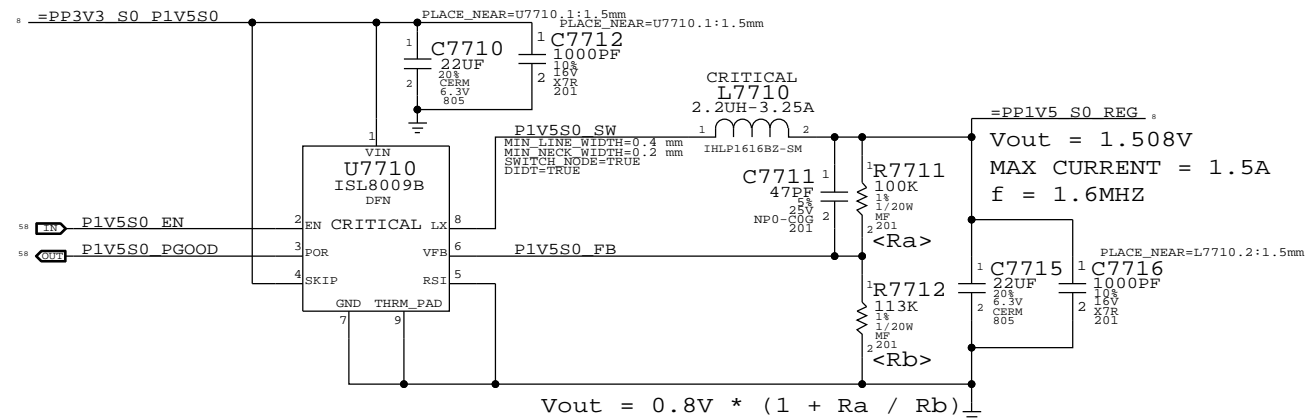


K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

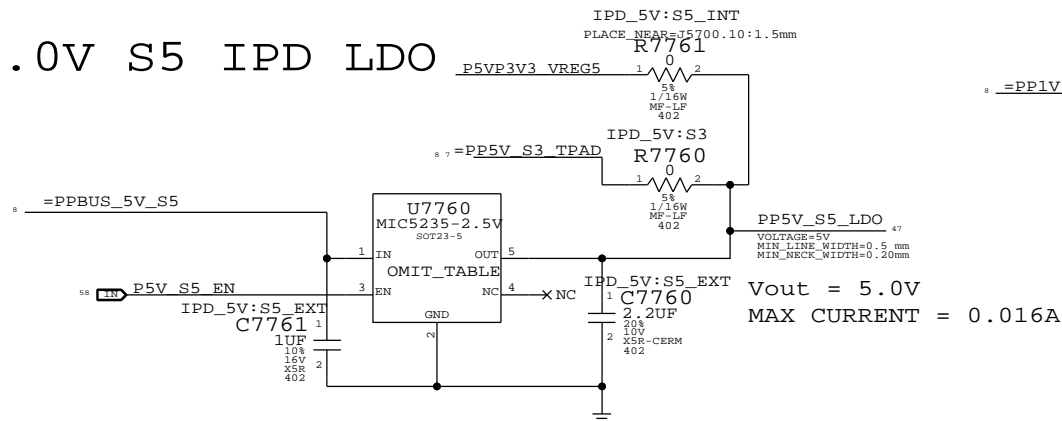
PAGE TITLE		PAGE NUMBER	
MCP VCore Regulator		051-8467	
Apple Inc.		3.3.0	
NOTICE OF PROPRIETARY PROPERTY:		75 OF 110	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		55 OF 74	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



1.5V S0 Regulator

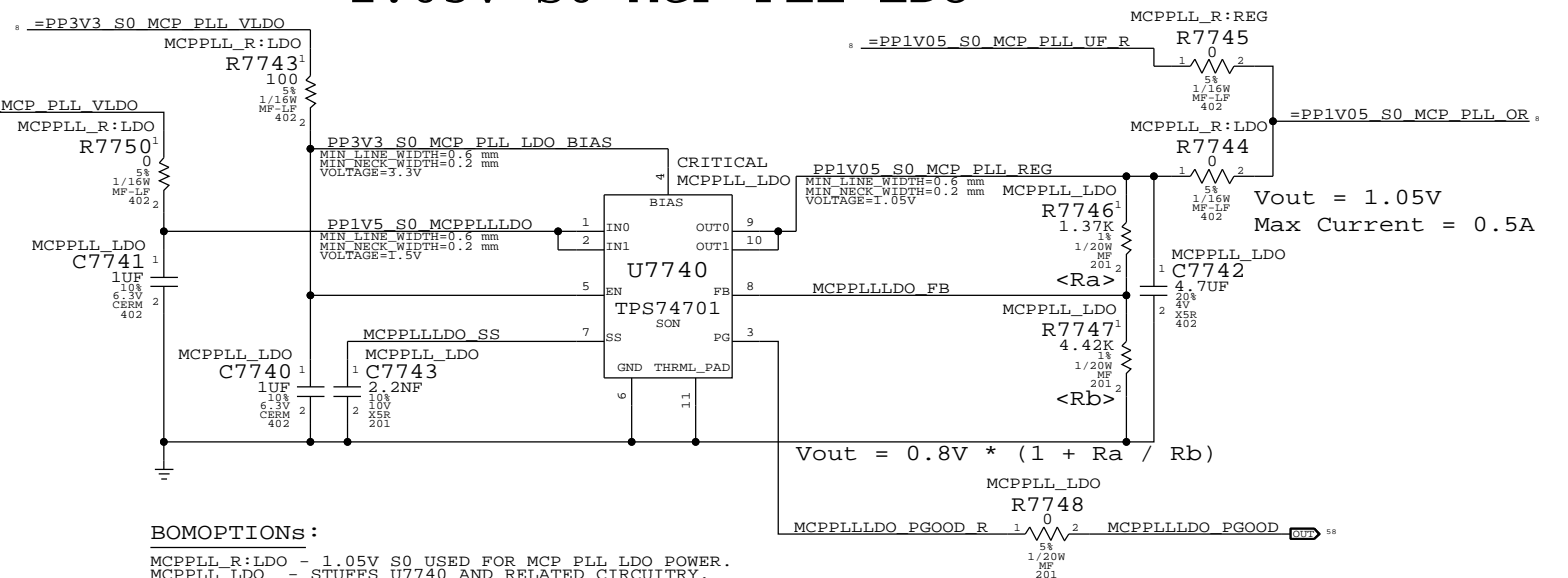


5.0V S5 IPD LDO



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3034	1	IC,LDO,MIC5235,5V,1A,150MA,SOT23-5	U7760		IPD_5V:S5_EXT

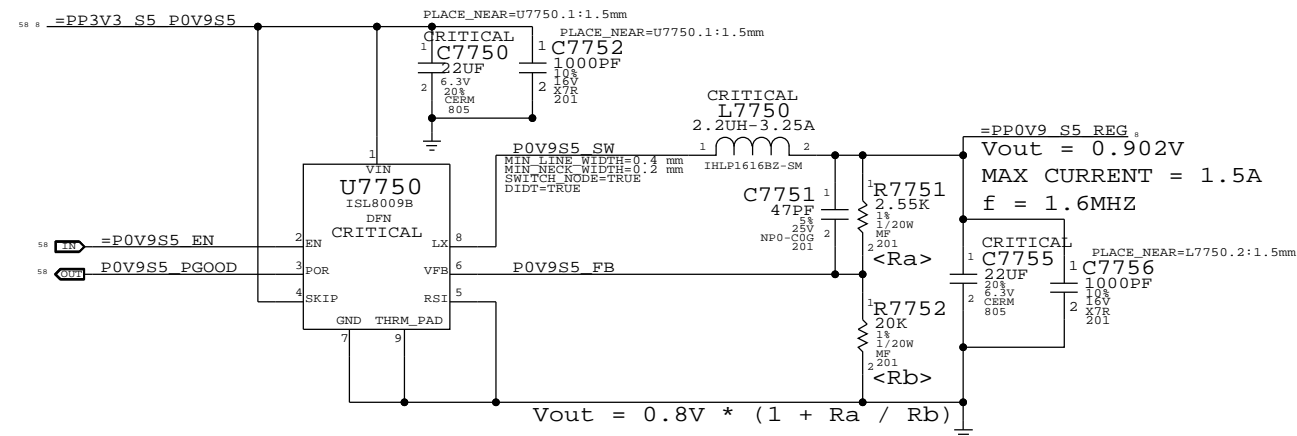
1.05V S0 MCP PLL LDO




BOMOPTIONS:

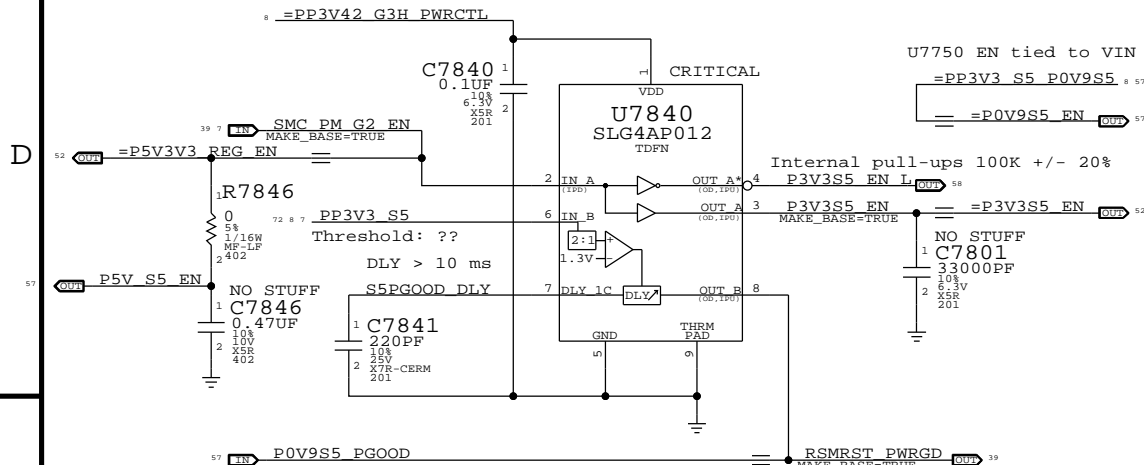
MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

MCP 0.9V S5 (AUXC) Switcher

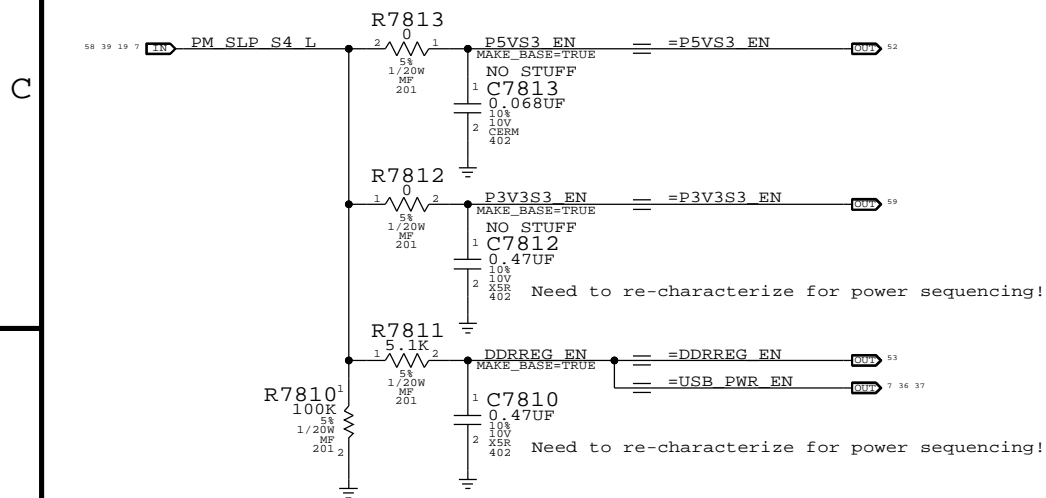


SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
Misc Power Supplies			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
		BRANCH	
		PAGE	77 OF 110
		SHEET	57 OF 74
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED			

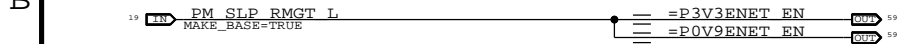
S5 Rail Enables & PGOOD



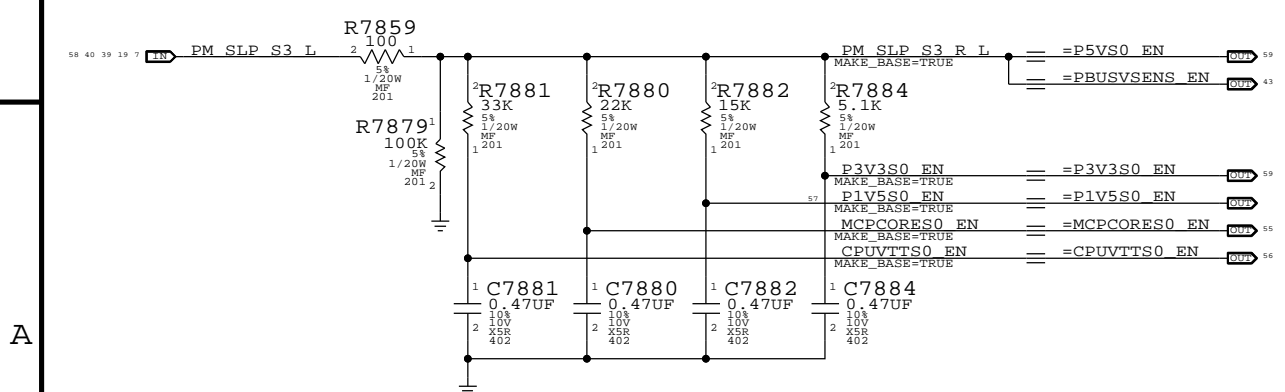
S3 Rail Enables



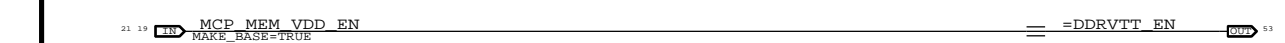
ENET Rail Enables



S0 Rail Enables

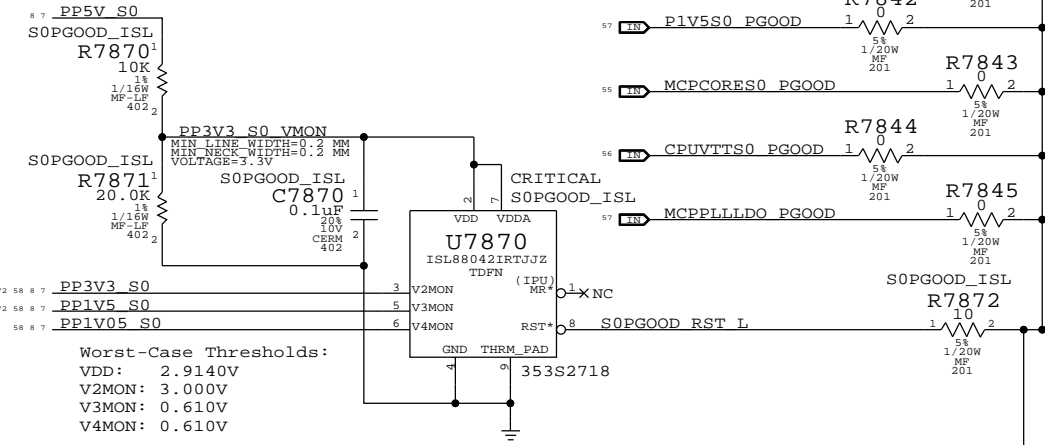


VTT Rail Enable

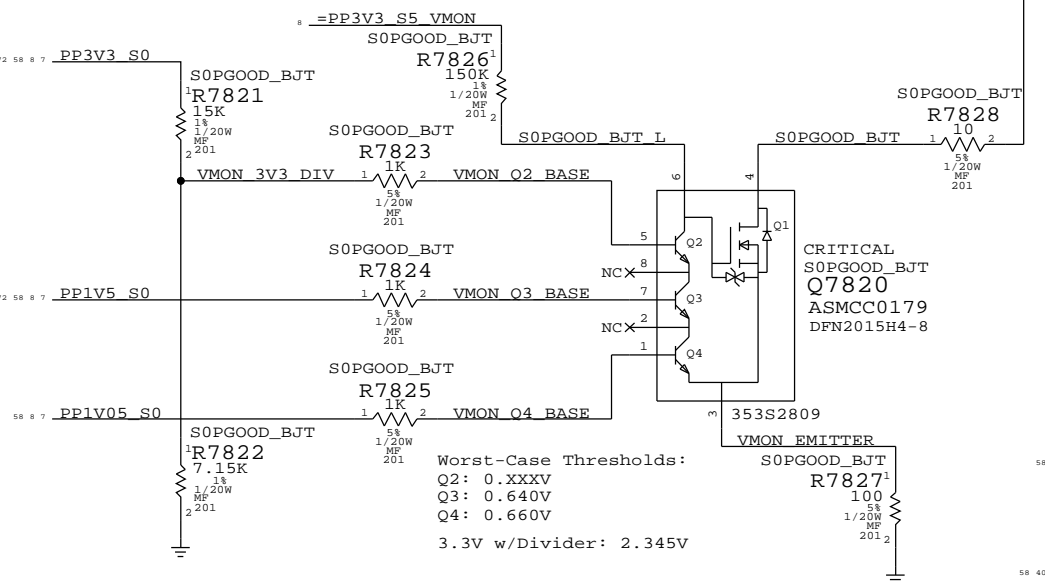


S0 Rail PGOOD Circuitry

S0 Rail PGOOD (ISL Version)



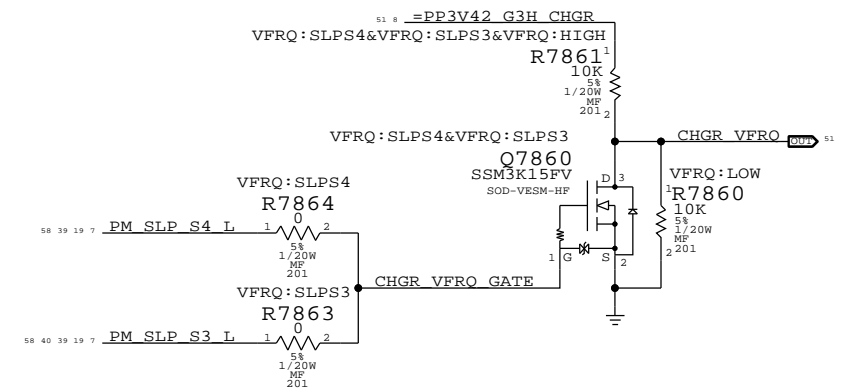
S0 Rail PGOOD (BJT Version)



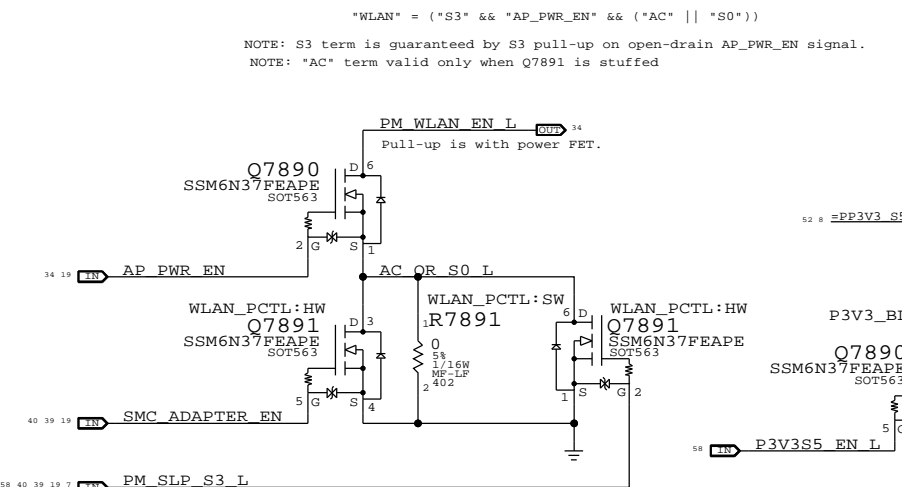
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

ISL6259 Frequency Select



WLAN Enable Generation



SYNC MASTER=K99 MLB

SYNC DATE=04/08/2010

Power Sequencing

Apple Inc.

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER

051-8467

REVISION

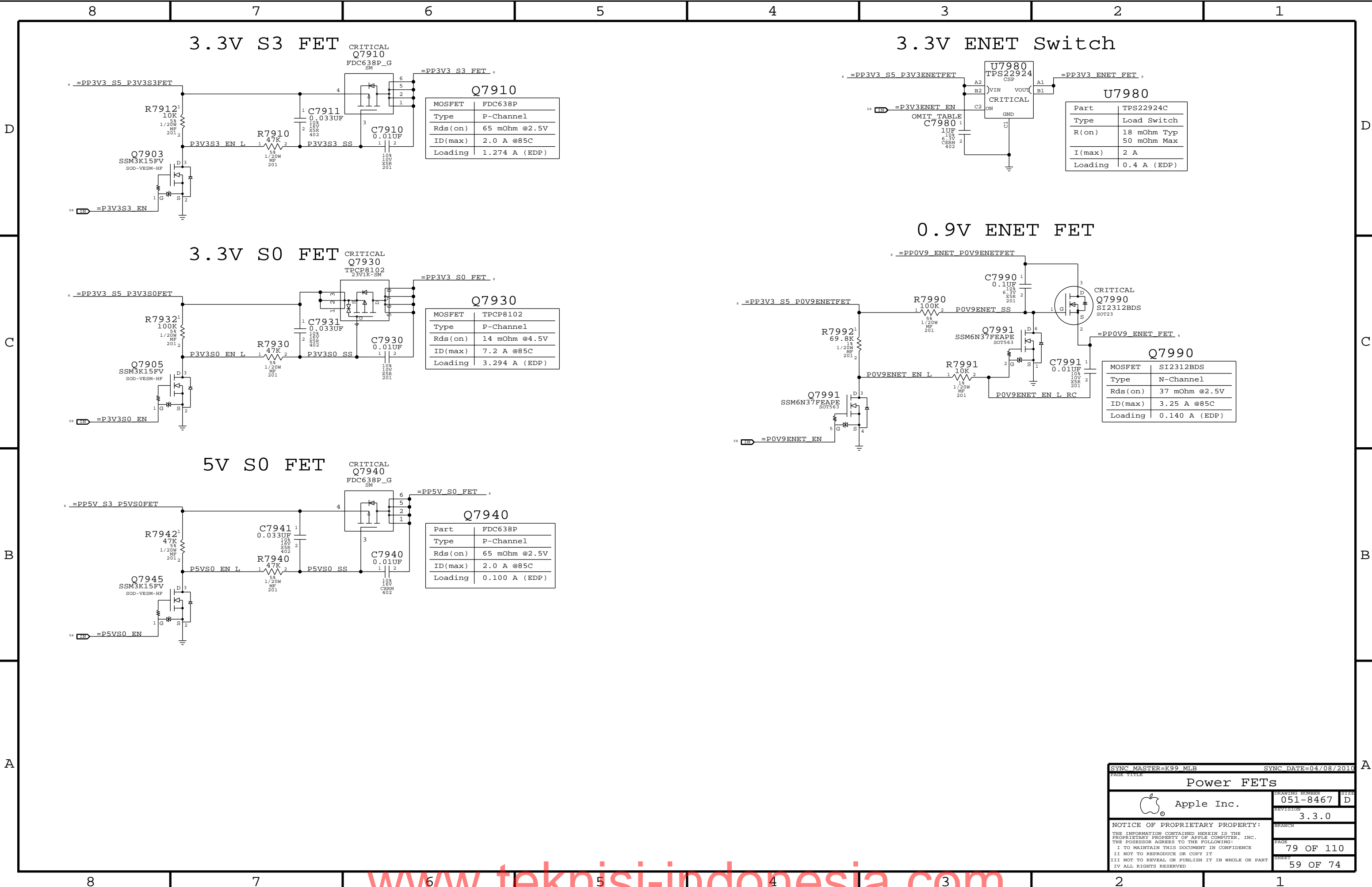
3.3.0

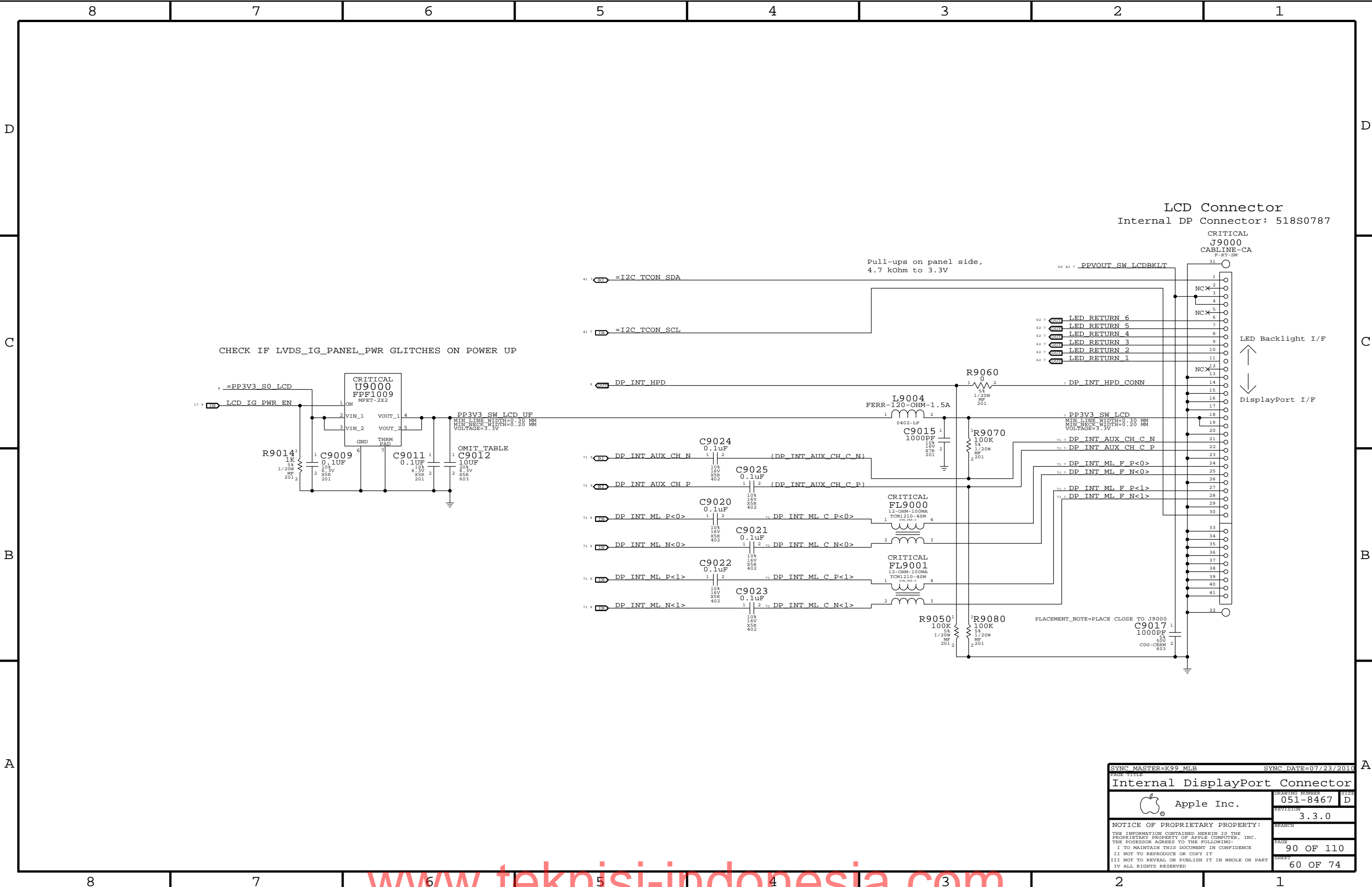
PAGE

78 OF 110

SHEET

58 OF 74






LCD Connector
Internal DP Connector: 518S0787

CRITICAL
J9000
CABLINE-CA
P-RT-SM

LED Backlight I/F
↑
↓
DisplayPort I/F

SYNC MASTER=K99 MLB		SYNC DATE=07/23/2010	
PAGE TITLE			
Internal DisplayPort Connector			
 Apple Inc.	DRAWING NUMBER		051-8467
	REVISION		3.3.0
	BRANCH		
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
PAGE		90	OF 110
SHEET		60	OF 74

Port Power Switch

CRITICAL
U9480
TPS2051B
SOT-23

CRITICAL
C9487
100UF
20V
POLY-TANT
CASE-B2-SM

CRITICAL
C9480
22UF
6.3V
X5R-201

CRITICAL
C9481
0.1UF
6.3V
X5R-201

CRITICAL
C9485
0.1UF
6.3V
X5R-201

CRITICAL
C9486
10UF
6.3V
X5R-603

PP3V3 SW DPILIM
MIN LINE WIDTH=0.50 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=3.3V
TP DPPWR OC L

L9400
FERR-120-OHM-3A

C9400
0.01UF
10V
X5R-201

PP3V3 SW DPPWR
MIN LINE WIDTH=0.50 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=3.3V

CRITICAL
DP_ESD
D9410
RCLAMP0524P
SLP2510P8

CRITICAL
FL9400
12-OHM-100MA
TCM1210-4SM

CRITICAL
FL9401
12-OHM-100MA
TCM1210-4SM

CRITICAL
FL9402
12-OHM-100MA
TCM1210-4SM

CRITICAL
DP_ESD
D9411
RCLAMP0524P
SLP2510P8

CRITICAL
DP_ESD
D9400
RCLAMP0504F
SC70-6-1

HDMI CEC
R9425
10K
1/20W
ME-2012

CRITICAL
J9400
MINIDSPYPT-K99
F-RT-TH

CRITICAL
DP_ESD
D9411
RCLAMP0524P
SLP2510P8

CRITICAL
DP_ESD
D9400
RCLAMP0504F
SC70-6-1

DP_EXT ML P<3> C9414
0.1UF
10V 6.3V X5R-201

DP_EXT ML N<3> C9415
0.1UF
10V 6.3V X5R-201

DP_EXT AUX CH C P

DP_EXT AUX CH C N

PP3V3 S0 DPCONN

PP5VR3V3 S0 DPCADET

R9443
100K
5V
1/20W
ME-2012

R9442
100K
5V
1/20W
ME-2012

DP_EXT CA DET

Q9440
2N7002DW-X-G
SOT-363

DP CA DET O L

NOTE: Q9440 must have Drain to Gate leakage of < 500 nA and gate to Source resistance of > 5 Mohm.

Q9440
2N7002DW-X-G
SOT-363

DP CA DET Q

R9422
1M
5V
1/20W
ME-2012

DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

CRITICAL
DP_ESD
D9400
RCLAMP0504F
SC70-6-1

PP3V3 SW DPILIM

R9444
10K
5V
1/20W
ME-2012

DP_EXT HPDI

Q9441
2N7002DW-X-G
SOT-363

DP_EXT HPDI L

Q9441
2N7002DW-X-G
SOT-363

DP HPDI Q

R9423
100K
5V
1/20W
ME-2012

DP Source must pull down HPDI input with greater than or equal to 100K (DPv1.1a).

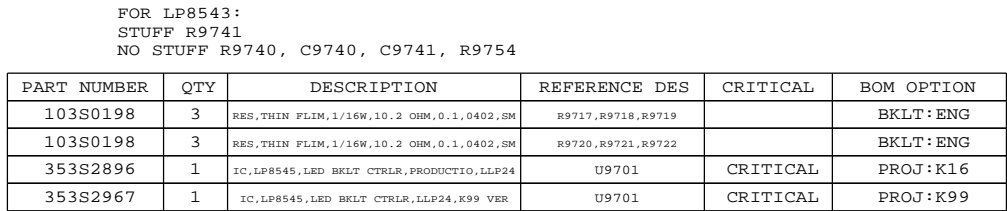
SYNC_MASTER=K16_MLB SYNC_DATE=06/01/2010


DisplayPort Connector

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BRANCHING NUMBER 051-8467
REVISION 3.3.0
PAGE 94 OF 110
SHEET 62 OF 74



SYNC MASTER=(K99 MLB)		SYNC DATE=(03/01/2010)	
PAGE TITLE			
LCD Backlight		Drawer	
 Apple Inc.		Drawing Number	Size
		051-8467	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1111 ALL RIGHTS RESERVED		REVISION	
		3	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1111 ALL RIGHTS RESERVED		BRANCH	
		PAGE	97 OF 110
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1111 ALL RIGHTS RESERVED		SHEET	
			63 OF 74

D

C

B

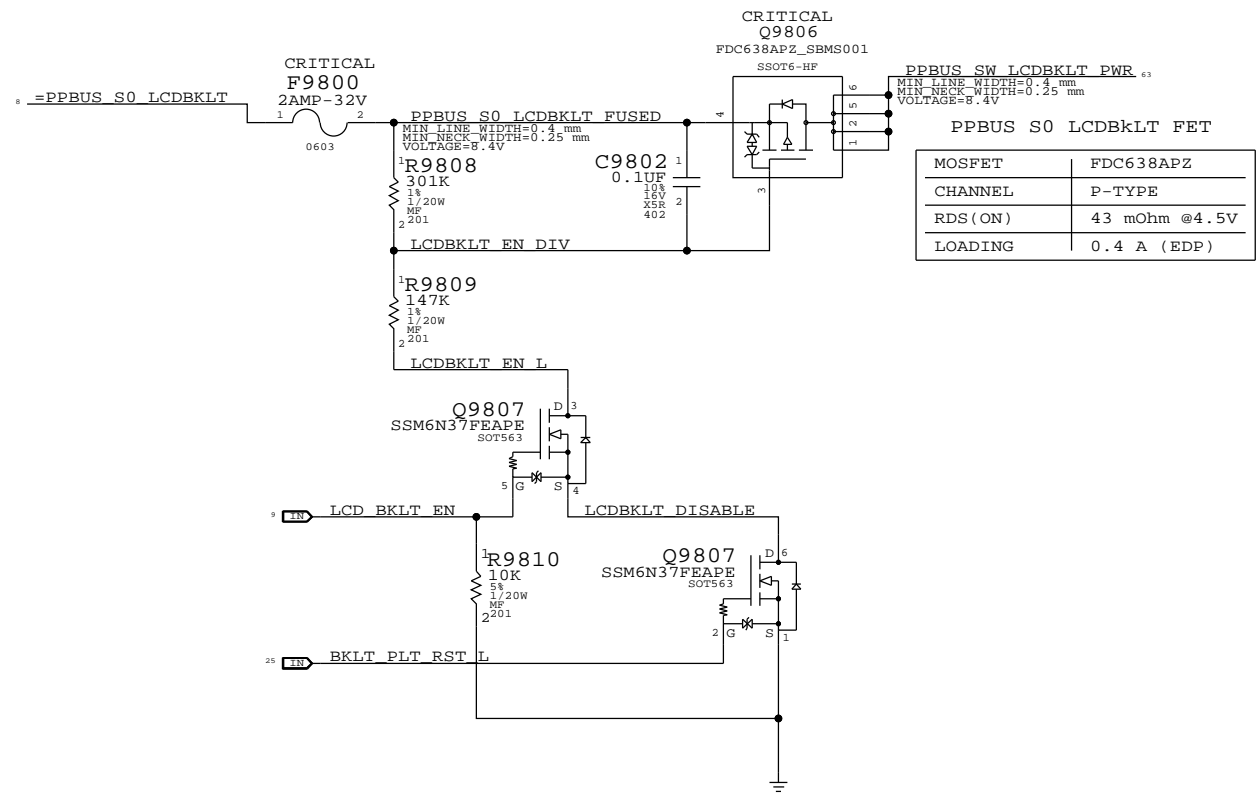
A

D

C

B


A



SYNC MASTER=K99 MLB

SYNC DATE=04/08/2010

LCD Backlight Support

 Apple Inc.

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER

051-8467

REVISION

3.3.0

BRANCH

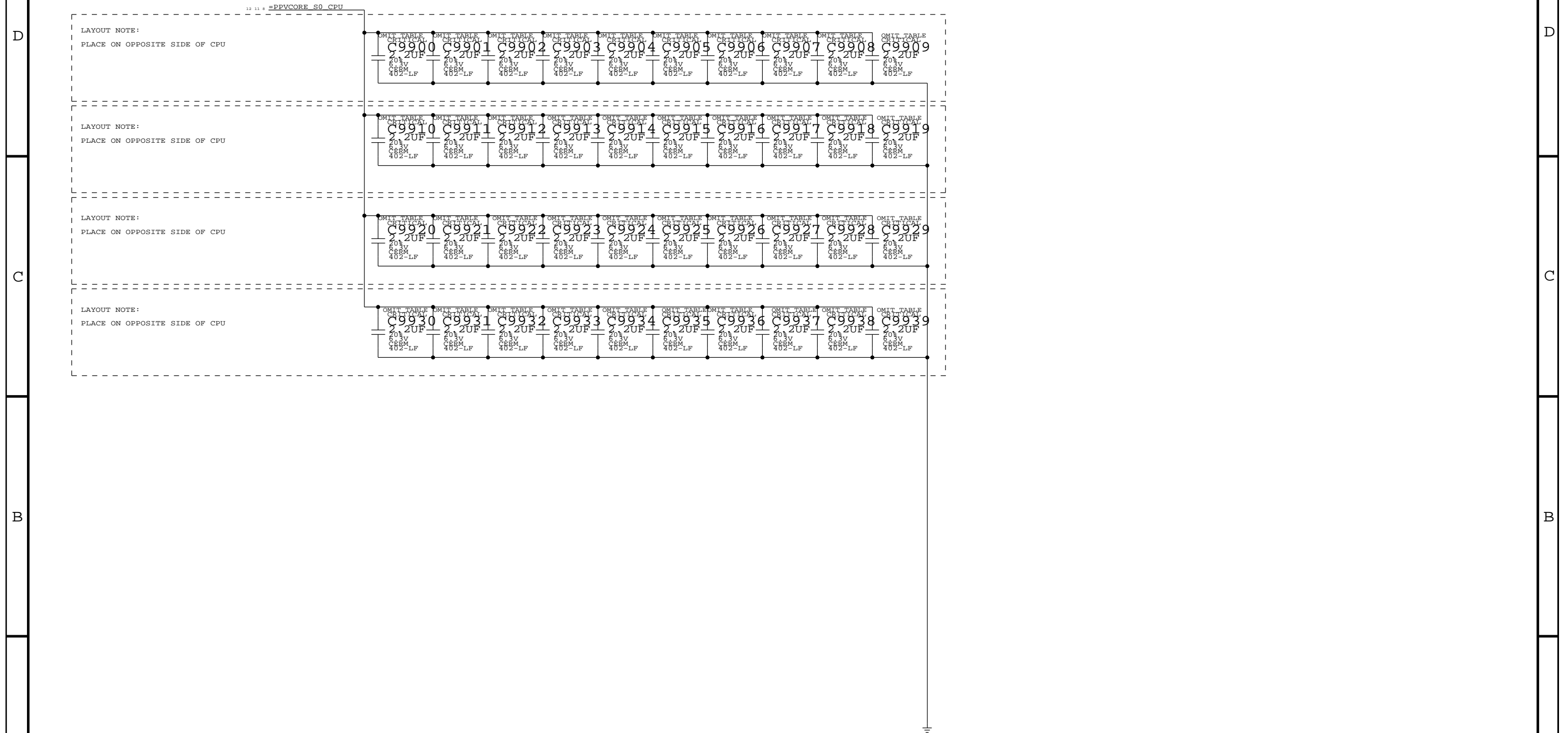
PAGE


98 OF 110

SHEET

64 OF 74

ADDITIONAL CPU VCORE HF DECOUPLING
40x 1uF 0402



SYNC MASTER=K99 MLB		SYNC DATE=05/18/2010	
PAGE 1 OF 1		PAGE 1 OF 1	
Additional CPU/GPU Decoupling			
 Apple Inc.		DRAWING NUMBER	051-8467
		SIZE	D
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE			
PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.			
THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		99 OF 110	
I NOT TO REPRODUCE OR COPY IT			
I WILL NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		SHEET	
I AM NOT TO REPRODUCE OR PUBLISH IT IN WHOLE OR PART		65 OF 74	

8

7

6

5

4

3

2

1

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB ADSTB L<1>	7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB ADS L	7 10 14
FSB_BREQ0_L	FSB_55S	FSB_1X	FSB BREQ0 L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB BNR L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB BPRI L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB DBSY L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB DEFER L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB DRDY L	10 14
FSB_1X	FSB_55S	FSB_1X	FSB HIT L	7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB HITM L	7 10 14
FSB_1X	FSB_55S	FSB_1X	FSB LOCK L	7 10 14
FSB_CPURST_L	FSB_55S	FSB_1X	FSB CPURST L	10 13 14
FSB_1X	FSB_55S	FSB_1X	FSB RS L<2..0>	10 14
FSB_1X	FSB_55S	FSB_1X	FSB TRDY L	10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU A20M L	10 14
CPU_BSEL	CPU_55S	CPU_AGTL	CPU BSEL<2..0>	9 10
CPU_FERR_L	CPU_55S	CPU_8MIL	CPU FERR L	10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU IGNE L	10 14
CPU_INIT_L	CPU_55S	CPU_AGTL	CPU INIT L	10 14
CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU INTR	10 14
CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU NMI	10 14
CPU_PROCHOT_L	CPU_55S	CPU_AGTL	CPU PROCHOT L	10 14 40
CPU_PWRGD	CPU_55S	CPU_AGTL	CPU PWRGD	10 13 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU SMI L	10 14
CPU_ASYNC	CPU_55S	CPU_AGTL	CPU STPCLK L	10 14
PM_THERMTRIP_L	CPU_55S	CPU_8MIL	PM THERMTRIP L	10 14 40
FSB_CPUSLP_L	CPU_55S	CPU_AGTL	FSB CPUSLP L	10 14
CPU_FROM_SR	CPU_55S	CPU_AGTL	CPU DPSLP L	10 14
CPU_DPRSTP_L	CPU_55S	CPU_AGTL	CPU DPRSTP L	10 14 54
CPU_ASYNC	CPU_55S	CPU_AGTL	FSB DPWR L	10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10 14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	13 14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	13 14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14
CPU_IERR_L	CPU_55S		CPU IERR L	10
PM_DPRSLPVR	CPU_55S	CPU_AGTL	PM DPRSLPVR	14 54
(See above)	CPU_55S	CPU_AGTL	IMVP DPRSLPVR	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10 33
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP TRST L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 13
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP CPURST L	13
	CPU_55S	CPU_8MIL	CPU VID<6..0>	11 12 54
	CPU_55S	CPU_8MIL	IMVP6 VID<6..0>	12
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11 54
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 54
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	54
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	54

8

7

6

5

4

3

2

1

www.teknisi-indonesia.com

8

7

6

5

4

3

2

1

SYNC MASTER=K99 MLB

SYNC DATE=04/08/2010

CPU/FSB Constraints

Apple Inc.

051-8467

3.3.0

100 OF 110

66 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_QS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 360 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
CMD/CTRL signals should be matched within 150 ps.
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

MEM_A/B_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK P<5..0>	9 15 26 27 32
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK N<5..0>	9 15 26 27 32
MEM_A_CKE	MEM_50S	MEM_CTRL	MEM A CKE<3..0>	15 21 26 27 32
MEM_A_CNTRL	MEM_50S	MEM_CTRL	MEM A CS L<3..0>	15 26 27 32
MEM_A_CNTRL	MEM_50S	MEM_CTRL	MEM A ODT<3..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A A<15..0>	9 15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A BA<2..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A RAS L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A CAS L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A WE L	15 26 27 32
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DM<0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DM<1>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DM<2>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DM<3>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	15 26
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	15 26
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK P<5..0>	9 15 28 29 32
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK N<5..0>	9 15 28 29 32
MEM_B_CKE	MEM_50S	MEM_CTRL	MEM B CKE<3..0>	15 21 28 29 32
MEM_B_CNTRL	MEM_50S	MEM_CTRL	MEM B CS L<3..0>	15 28 29 32
MEM_B_CNTRL	MEM_50S	MEM_CTRL	MEM B ODT<3..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B A<15..0>	9 15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B BA<2..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B RAS L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B CAS L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B WE L	15 28 29 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	15

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
Memory Constraints			
 Apple Inc.	DRAWING NUMBER	051-8467	SIZE D
	REVISION	3.3.0	
	BRANCH		
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED			
		PAGE 101 OF 110	SHEET 67 OF 74

PCI-Express

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

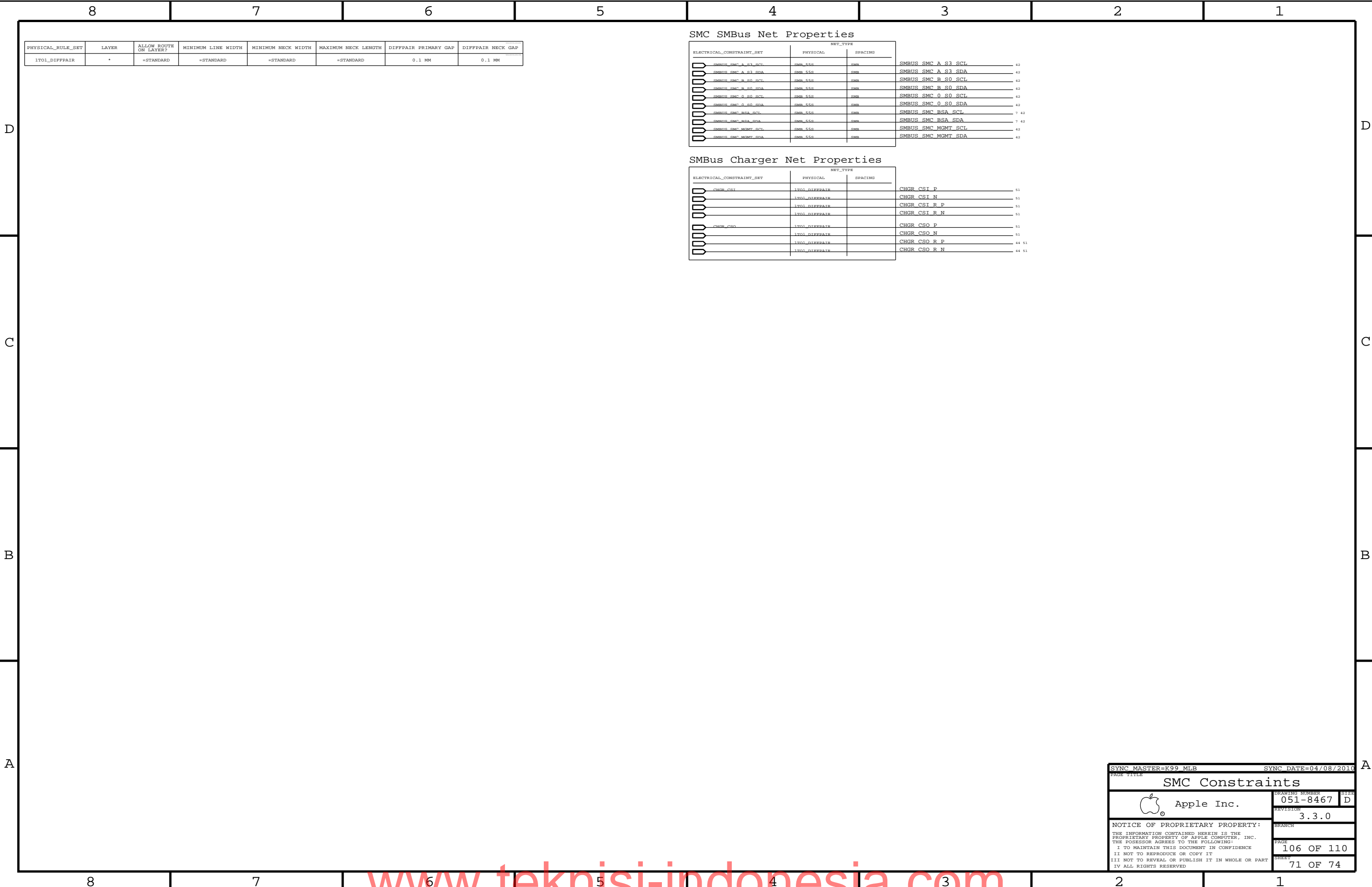
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERM_P	*	8 MIL	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	PCIE_90D	PCIE	PEG R2D P<15..0>
	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
	PCIE_90D	PCIE	PEG D2R N<15..0>
	PCIE_90D	PCIE	PEG D2R C P<15..0>
	PCIE_90D	PCIE	PEG D2R C N<15..0>
	PCIE_90D	PCIE	PCIE AP R2D P
	PCIE_90D	PCIE	PCIE AP R2D N
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C P
	PCIE_90D	PCIE	PCIE AP R2D C N
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R P
	PCIE_90D	PCIE	PCIE AP D2R N
	PCIE_90D	PCIE	PCIE ENET R2D P
	PCIE_90D	PCIE	PCIE ENET R2D N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C P
	PCIE_90D	PCIE	PCIE ENET R2D C N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R P
	PCIE_90D	PCIE	PCIE ENET D2R N
	PCIE_90D	PCIE	PCIE ENET D2R C P
	PCIE_90D	PCIE	PCIE ENET D2R C N
	PCIE_90D	PCIE	PCIE FW R2D P
	PCIE_90D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P
	PCIE_90D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P
	PCIE_90D	PCIE	PCIE FW D2R N
	PCIE_90D	PCIE	PCIE FW D2R C P
	PCIE_90D	PCIE	PCIE FW D2R C N
MCP_PEO_REECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
MCP_PE1_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP N
MCP_PE2_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N
MCP_PE3_REECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP PEX0 TERMP
CRT_RED	CRT_50S	CRT	CRT IG R C PR
CRT_GREEN	CRT_50S	CRT	CRT IG G Y Y
CRT_BLUE	CRT_50S	CRT	CRT IG B COMP PB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC
CRT_VSYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC
MCP_DAC_RSET		MCP_DAC_COMP	MCP TV DAC RSET
MCP_DAC_VREF		MCP_DAC_COMP	MCP TV DAC VREF
DP_INT_ML	DP_90D	DISPLAYPORT	DP IG ML1 P<1..0>
DP_INT_ML	DP_90D	DISPLAYPORT	DP IG ML1 N<1..0>
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH1 P
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH1 N
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML0 P<3..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML0 N<3..0>
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH0 P
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH0 N
MCP_TMDS0_RSET	MCP_DV_COMP		MCP TMDS0 RSET
MCP_TMDS0_VPROBE			MCP TMDS0 VPROBE
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA P<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK P
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA P<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA N<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP IFPAB RSET
MCP_IFPAB_VPROBE			MCP IFPAB VPROBE
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P
	SATA_90D	SATA	SATA HDD R2D C N
	SATA_90D	SATA	SATA HDD R2D P
	SATA_90D	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P
	SATA_90D	SATA	SATA HDD D2R N
	SATA_90D	SATA	SATA HDD D2R C P
	SATA_90D	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P
	SATA_90D	SATA	SATA ODD R2D C N
	SATA_90D	SATA	SATA ODD R2D P
	SATA_90D	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P
	SATA_90D	SATA	SATA ODD D2R N
	SATA_90D	SATA	SATA ODD D2R C P
	SATA_90D	SATA	SATA ODD D2R C N
MCP_SATA_TERMP		SATA_TERMP	MCP SATA TERMP

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
MCP Constraints 1			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8467		D
	REVISION		
		3.3.0	
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED			
BRANCH			
PAGE		102 OF 110	
SHEET		68 OF 74	



PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=1:1_SPACING	?
AUDIO	*	=1:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SD CARD READER LAYOUT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_5S5 OVERRIDE	* OVERRIDE	OVERRIDE	=STANDARD OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	(USB_EXTN)	USB_90D	USB	USB_EXTN_MUXED_P	36 69
	(USB_EXTN)	USB_90D	USB	USB_EXTN_MUXED_N	36 69
	(USB_EXTN)	USB_90D	USB	USB_LT1_P	36
	(USB_EXTN)	USB_90D	USB	USB_LT1_N	36
	(USB_TPAD)	USB_90D	USB	USB_TPAD_P	18 47 69
	(USB_TPAD)	USB_90D	USB	USB_TPAD_N	18 47 69
	(USB_TPAD)	USB_90D	USB	USB_TPAD_CONN_P	7 47
	(USB_TPAD)	USB_90D	USB	USB_TPAD_CONN_N	7 47
	SMR510_SMC_MCMPT_SDA	SMR_55S	SMR	I2C_SMC_SMS_SDA_R	
	SMR510_SMC_MCMPT_SCL	SMR_55S	SMR	I2C_SMC_SMS_SCL_R	
		SMR_55S	SMR	I2C_TCON_SCL	42
		SMR_55S	SMR	I2C_TCON_SDA	42
		SMR_55S	SMR	I2C_TCON_SCL_CONN	60
		SMR_55S	SMR	I2C_TCON_SDA_CONN	60





Graphics Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	DP_90D	DISPLAYPORT	DP INT ML P<1..0>	9 60
	DP_90D	DISPLAYPORT	DP INT ML N<1..0>	9 60
	DP_90D	DISPLAYPORT	DP INT ML C P<1..0>	60
	DP_90D	DISPLAYPORT	DP INT ML C N<1..0>	60
	DP_90D	DISPLAYPORT	DP INT ML F P<1..0>	7 60
	DP_90D	DISPLAYPORT	DP INT ML F N<1..0>	7 60
	DP_90D	DISPLAYPORT	DP INT AUX CH C P	7 60
	DP_90D	DISPLAYPORT	DP INT AUX CH C N	7 60
	DP_90D	DISPLAYPORT	DP INT AUX CH P	9 60
	DP_90D	DISPLAYPORT	DP INT AUX CH N	9 60
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML P<3..0>	9 62
	DP_90D	DISPLAYPORT	DP EXT ML N<3..0>	9 62
	DP_90D	DISPLAYPORT	DP EXT ML C P<3..0>	62
	DP_90D	DISPLAYPORT	DP EXT ML C N<3..0>	62
	DP_90D	DISPLAYPORT	DP EXT ML F P<3..0>	62
	DP_90D	DISPLAYPORT	DP EXT ML F N<3..0>	62
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP EXT AUX CH C P	9 62
	DP_90D	DISPLAYPORT	DP EXT AUX CH C N	9 62

Power Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	CPU1THMSNS_D2	THERM 1T01 55S	THERM	DRAMTHMSNS D2 P	45
		THERM 1T01 55S	THERM	DRAMTHMSNS D2 N	45
	CPU_THERMD	THERM 1T01 55S	THERM	CPU_THERMD P	10 45
		THERM 1T01 55S	THERM	CPU_THERMD N	10 45
	MCPTHMSNS_D2	THERM 1T01 55S	THERM	MLBR_THMDIODE P	45
		THERM 1T01 55S	THERM	MLBR_THMDIODE N	45
	MCP_THMDIODE	THERM 1T01 55S	THERM	MCP_THMDIODE P	19 45
		THERM 1T01 55S	THERM	MCP_THMDIODE N	19 45
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS 1V5_S3 P	43 53
		SENSE 1T01 55S	SENSE	ISNS 1V5_S3 N	43 53
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS AIRPORT P	34 43
		SENSE 1T01 55S	SENSE	ISNS AIRPORT N	34 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS CSREG P	44
		SENSE 1T01 55S	SENSE	ISNS CSREG N	44
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS HDD P	35 43
		SENSE 1T01 55S	SENSE	ISNS HDD N	35 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS LCDBKLT P	43 43
		SENSE 1T01 55S	SENSE	ISNS LCDBKLT N	43 43
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	CPUVTT50_CS P	56
		SENSE 1T01 55S	SENSE	CPUVTT50_CS N	56
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	IMVP6_CS P	54
		SENSE 1T01 55S	SENSE	IMVP6_CS N	54
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	IMVP6_CS_R P	54
		SENSE 1T01 55S	SENSE	IMVP6_CS_R N	54
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	CPU_VTTSense P	56
		SENSE 1T01 55S	SENSE	CPU_VTTSense N	56
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	MCPCORE50_VSEN P	22 55
		SENSE 1T01 55S	SENSE	MCPCORE50_VSEN N	22 55
			MEM_POWER	PP1V5R1V35_S3	7 8
			SB_POWER	PP3V3_S5	7 8 58
			SB_POWER	PP3V3_S0	7 8 58
			SB_POWER	PP1V5_S0	7 8 58
			GND	GND	

Audio Net Properties

		NET_TYPE			
ELECTRICAL_CONSTRAINT_SET		PHYSICAL	SPACING		
	SPKRAMP_INR	DIEFFPAIR	AUDIO	SPKRAMP_INR_P	7 37 49
		DIEFFPAIR	AUDIO	SPKRAMP_INR_N	7 37 49
	MAX98300_R	DIEFFPAIR	AUDIO	MAX98300_R_P	49
		DIEFFPAIR	AUDIO	MAX98300_R_N	49

K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL3, ISL10	Y	0.250 MM	0.250 MM			
27P4_OHM_SE	ISL4, ISL9	Y	0.250 MM	0.250 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE ISL3, ISL4, ISL9, ISL10		Y	0.140 MM	0.140 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE ISL3, ISL4, ISL9, ISL10		Y	0.090 MM	0.090 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE ISL3, ISL4, ISL9, ISL10		Y	0.076 MM	0.076 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.125 MM	0.125 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
75_OHM_DIFF	TOP,BOTTOM	Y	0.160 MM	0.160 MM		0.160 MM	0.160 MM
75_OHM_DIFF	ISL3,ISL10	Y	0.120 MM	0.120 MM		0.140 MM	0.140 MM
75_OHM_DIFF	ISL4,ISL9	Y	0.140 MM	0.140 MM		0.140 MM	0.140 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
95_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
95_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL3,ISL10	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM
100_OHM_DIFF	ISL4,ISL9	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPIV5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	= STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
1.5X_DIELECTRIC	*	0.105 MM	?
5X_DIELECTRIC	*	0.350 MM	?

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TYPE		K99 RULE DEFINITIONS	
 Apple Inc.		DRAWING NUMBER 051-8467	SIZE D
		REVISION 3.3.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		PAGE 109 OF 110	
		SHEET 73 OF 74	


8		7		6		5		4		3		2		1			
1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS																	
SAMSUNG						MURATA						TAIYO YUDEN					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	2	CAP, 1UF, 6.3V, 10%, 0402	CT003,CT060	CRITICAL	SS_CAP_1UF	138S0628	2	CAP, 1UF, 6.3V, 10%, 0402	CT003,CT060	CRITICAL	MU_CAP_1UF	138S0630	2	CAP, 1UF, 6.3V, 10%, 0402	CT003,CT060	CRITICAL	TY_CAP_1UF
2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS																	
SAMSUNG						MURATA						TAIYO YUDEN					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1246,C1246,C1247,C1247,C1248,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1246,C1246,C1247,C1247,C1248,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1246,C1246,C1247,C1247,C1248,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1261,C1262,C1263,C1264,C1266,C1266,C1267,C1267,C1268,C1268	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1261,C1262,C1263,C1264,C1266,C1266,C1267,C1267,C1268,C1268	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1261,C1262,C1263,C1264,C1266,C1266,C1267,C1267,C1268,C1268	CRITICAL	TY_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1269,C1269,C1269,C1269,C1269,C1269,C1269,C1269	CRITICAL	SS_CAP_2_2UF	138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1269,C1269,C1269,C1269,C1269,C1269,C1269,C1269	CRITICAL	MU_CAP_2_2UF	138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1269,C1269,C1269,C1269,C1269,C1269,C1269,C1269	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0901,C0902,C0903,C0904,C0905,C0906,C0907,C0907	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0901,C0902,C0903,C0904,C0905,C0906,C0907,C0907	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0901,C0902,C0903,C0904,C0905,C0906,C0907,C0907	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0911,C0912,C0913,C0914,C0915,C0916,C0917,C0917	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0911,C0912,C0913,C0914,C0915,C0916,C0917,C0917	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0911,C0912,C0913,C0914,C0915,C0916,C0917,C0917	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0921,C0922,C0923,C0924,C0925,C0926,C0927,C0927	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0921,C0922,C0923,C0924,C0925,C0926,C0927,C0927	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0921,C0922,C0923,C0924,C0925,C0926,C0927,C0927	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0931,C0932,C0933,C0934,C0935,C0936,C0937,C0937	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0931,C0932,C0933,C0934,C0935,C0936,C0937,C0937	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C0931,C0932,C0933,C0934,C0935,C0936,C0937,C0937	CRITICAL	TY_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1289,C1289,C1287,C1288,C1291,C1292,C1293,C1293	CRITICAL	SS_CAP_2_2UF	138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1289,C1289,C1287,C1288,C1291,C1292,C1293,C1293	CRITICAL	MU_CAP_2_2UF	138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1289,C1289,C1287,C1288,C1291,C1292,C1293,C1293	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1301,C1304,C1305,C1310,C1311,C1312,C1314,C1314	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1301,C1304,C1305,C1310,C1311,C1312,C1314,C1314	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1301,C1304,C1305,C1310,C1311,C1312,C1314,C1314	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1321,C1324,C1325,C1330,C1331,C1334,C1335,C1335	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1321,C1324,C1325,C1330,C1331,C1334,C1335,C1335	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1321,C1324,C1325,C1330,C1331,C1334,C1335,C1335	CRITICAL	TY_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1343,C1344,C1345,C1346,C1350,C1351,C1354,C1354	CRITICAL	SS_CAP_2_2UF	138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1343,C1344,C1345,C1346,C1350,C1351,C1354,C1354	CRITICAL	MU_CAP_2_2UF	138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1343,C1344,C1345,C1346,C1350,C1351,C1354,C1354	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1361,C1364,C1365,C1370,C1371,C1372,C1374,C1374	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1361,C1364,C1365,C1370,C1371,C1372,C1374,C1374	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1361,C1364,C1365,C1370,C1371,C1372,C1374,C1374	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1371,C1374,C1375,C1380,C1381,C1384,C1385,C1385	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1371,C1374,C1375,C1380,C1381,C1384,C1385,C1385	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1371,C1374,C1375,C1380,C1381,C1384,C1385,C1385	CRITICAL	TY_CAP_2_2UF
138S0632	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1392,C1394,C1395,C1396,C1399,C1401,C1404,C1405	CRITICAL	SS_CAP_2_2UF	138S0633	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1392,C1394,C1395,C1396,C1399,C1401,C1404,C1405	CRITICAL	MU_CAP_2_2UF	138S0634	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1392,C1394,C1395,C1396,C1399,C1401,C1404,C1405	CRITICAL	TY_CAP_2_2UF
10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS																	
SAMSUNG						MURATA						TAIYO YUDEN					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	SS_CAP_10UF	138S0625	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	MU_CAP_10UF	138S0627	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	TY_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C0605,C0609,C0620,C7209,C7209,C7345,C7345,C7345,C7345	CRITICAL	SS_CAP_10UF	138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C0605,C0609,C0620,C7209,C7209,C7345,C7345,C7345,C7345	CRITICAL	MU_CAP_10UF	138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C0605,C0609,C0620,C7209,C7209,C7345,C7345,C7345,C7345	CRITICAL	TY_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C0611,C0616,C0620,C0620,C0660,C0667,C0667,C0667	CRITICAL	SS_CAP_10UF	138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C0611,C0616,C0620,C0620,C0660,C0667,C0667,C0667	CRITICAL	MU_CAP_10UF	138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C0611,C0616,C0620,C0620,C0660,C0667,C0667,C0667	CRITICAL	TY_CAP_10UF
22UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS																	
SAMSUNG						MURATA						TAIYO YUDEN					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0635	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	SS_CAP_22UF	138S0676	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	MU_CAP_22UF	138S0688	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	TY_CAP_22UF
138S0635	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	SS_CAP_22UF	138S0676	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	MU_CAP_22UF	138S0688	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	TY_CAP_22UF
138S0635	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	SS_CAP_22UF	138S0676	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	MU_CAP_22UF	138S0688	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	TY_CAP_22UF
Acoustic Cap BOM Config Tables																	
Apple Inc.																	
NOTICE OF PROPRIETARY PROPERTY:																	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:																	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE																	
II NOT TO REPRODUCE OR COPY IT																	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART																	
IV ALL RIGHTS RESERVED																	
www.teknisi-indonesia.com																	

SYNC MASTER=K16 MLB

SYNC DATE=06/01/2010

PAGE TITLE

Acoustic Cap BOM Config Tables

 Apple Inc.

DRAWING NUMBER
051-8467

REVISION
3.3.0

BRANCH

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PAGE
110 OF 110

SHEET
74 OF 74